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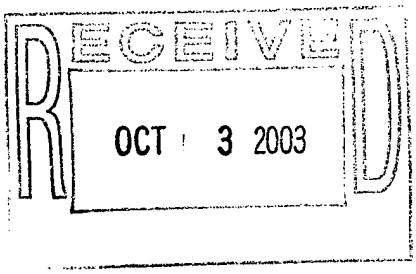
Applicant: Adrian P. Wise et al. Attorney Richard Stokey, Esq.
Serial No.: 09/770,157 Docket No.: 94100412(EP)USC1X1C1D1 PDDD
Filed: January 26, 2001 Confirmation No. 8565
For: MULTISTANDARD VIDEO DECODER AND DECOMPRESSION SYSTEM FOR PROCESSING ENCODED BIT STREAMS INCLUDING START CODE DETECTION AND METHODS RELATING THERETO

1. Transmittal Form;
2. Fee Transmittal;
3. Amendment Transmittal;
4. Amendment (Page 1 - 16);
5. Terminal Disclaimer to Obviate Patenting Rejection Over A Prior Patent;
6. Replacement Sheets, Specification Pgs. 36 – 50;
7. Replacement Sheets, Tables A.11, A.14 and A.17;
8. Resubmitting Foreign Patent/Published Foreign Patent Applications and Other Documents as mentioned in the IDS filed on 1/26/01 and per Office Communication dated 6/30/03;
9. Cover Letter;
10. Pre-Paid Postcard, Control No. 5DZS7N; and
11. Certificate of Express Mail No. CD19299326KUS, dated September 24, 2003.



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September 24, 2003

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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CUSTOMER NUMBER
22887
PATENT TRADEMARK OFFICE

Re: U.S. Application No.: 09/770,157
Filed: January 26, 2001
Confirmation No. 8565
Entitled: MULTISTANDARD VIDEO DECODER AND DECOMPRESSION SYSTEM FOR PROCESSING ENCODED BIT STREAMS INCLUDING START CODE DETECTION AND METHODS RELATING THERETO
Inventor(s): Adrian P. Wise et al.
Our File No.: 94100412(EP)USC1X1C1D1 PDDD

Dear Sir:

Enclosed for filing in the above-referenced patent are the following documents:

1. Transmittal Form;
2. Fee Transmittal;
3. Amendment Transmittal;
4. Amendment (Page 1 - 16);
5. Terminal Disclaimer to Obviate Patenting Rejection Over A Prior Patent;
6. Replacement Sheets, Specification Pgs. 36 – 50;
7. Replacement Sheets, Tables A.11, A.14 and A.17;
8. Resubmitting Foreign Patent/Published Foreign Patent Applications and Other Documents as mentioned in the IDS filed on 1/26/01 and per Office Communication dated 6/30/03;
9. Cover Letter;
10. Pre-Paid Postcard, Control No. 5DZS7N, and
11. Certificate of Express Mail No. CD19299326KUS, dated September 24, 2003.

Please indicate on the enclosed postcard the date of receipt of the enclosed materials and mail this pre-paid postcard to acknowledge receipt of this transmittal.

Very truly yours,

DISCOVISION ASSOCIATES

Richard Stokey
Patent Prosecution Attorney
INTELLECTUAL PROPERTY DEVELOPMENT

FILING OF CORRESPONDENCE BY EXPRESS MAIL UNDER 37 C.F.R. § 1.10

CD 19299326 KUS 9/24/03
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RS:cs

Enclosures

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PTO/SB/21 (05-03)
Approved for use through 04/30/2003. OMB 0651-0031
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/770,157
Filing Date	January 26, 2001
First Named Inventor	Adrian P. Wise, et al.
Art Unit	2154
Examiner Name	Dustin Nguyen
Total Number of Pages in This Submission	
Attorney Docket Number	94100412(EP)USC1X1C1D1 PDDD

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ENCLOSURES (check all that apply)

- [X] Fee Transmittal Form
- [ ] Fee Attached
- [X] Amendment / Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [X] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) (please identify below):

Cover Letter, and
Certificate of Express Mail.

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	**DISCOVISION ASSOCIATES -- Intellectual Property Development** **2355 Main Street, Suite 200, Irvine, CA 92614 -- U.S.A. -- Tel: (949) 660-5000**
Signature	
Date	September 24, 2003

CERTIFICATE OF TRANSMISSION / MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

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Typed or printed name	Colleen A. Smothers		
Signature		Date	September 24, 2003

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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AMENDMENT TRANSMITTAL LETTER

Attorney Docket No. 94100412(EP)USC1X1C1D1 PDDD

Confirmation No.: 8565

SERIAL NO. 09/770,157	FILING DATE 1/26/2001	EXAMINER Dustin Nguyen	Group Art Unit 2154

INVENTION: MULTISTANDARD VIDEO DECODER AND DECOMPRESSION SYSTEM FOR PROCESSING ENCODED BIT STREAMS INCLUDING START CODE DETECTION AND METHODS RELATING THERETO

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TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is an amendment in the above-identified application. The fee has been calculated as shown below.

CLAIMS AS AMENDED — Large Entity

(1)	(2) Claims Remaining After Amendment	(3)	(4) Highest No. Previously Paid for	(5) No. of Extra Claims Present	(6) RATE	(7) FEE CODES	(8) ADDITIONAL FEE
Total Claims	* 29	Minus	** 29 =	0	X $18	1202	= 0
Indep. Claims	* 4	Minus	*** 4 =	0	X $84	1201	= 0
Multiple Dep. Claims		Minus			$280	1203	=

TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

* If the entry in column 2 is less than the entry in column 4, write "0" in column 5.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

( ) No additional fee is required.

( ) A check in amount of $_____.00 is attached.

(X) Please charge any additional fees or credit overpayment to Deposit Account No. 04-1175. The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 04-1175.

(X) Any patent application processing fees under 37 CFR 1.17.

(X) Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Date: Sept. 24, 2003

Richard J. Stokey
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94100412(EP)USC1X1C1D1 PDDD
USSN: 09/770,157

PATENT
Art Group: 2154

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	§	
	§	
Adrian P. Wise et al.	§	Confirmation No. 8565
	§	
Filed: January 26, 2001	§	Art Unit: 2154
	§	
Serial No.: 09/770,157	§	Examiner: Dustin Nguyen
	§	
For: MULTISTANDARD VIDEO DECODER AND DECOMPRESSION SYSTEM FOR PROCESSING ENCODED BIT STREAMS INCLUDING START CODE DETECTION AND METHODS RELATING THERETO	§	Attorney Docket No. 94100412(EP)USC1X1C1D1 PDDD

AMENDMENT

Mail Stop Non-Fee Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

FILING OF CORRESPONDENCE BY EXPRESS MAIL UNDER 37 C.F.R. § 1.10

CD 19299326 KUS *9/24/03*
Express Mail Label Number *Date of Deposit*

In response to the outstanding Office Action of June 30, 2003, please amend the above-identified patent application as follows:

Amendments to the Specification

Please replace the Abstract of page 675 with the new Abstract which is submitted herein on a separate piece of paper as required by 37 CFR 1.72.

Please replace the paragraph beginning on page 1, lines 2-8, with the following rewritten paragraph:

CROSS REFERENCE TO RELATED APPLICATIONS
This application is a divisional of U.S. Serial No. 09/307, 239 filed October 7, 1997, issued as U.S. Patent No. 6,330,666, which is a continuation of U.S. Ser. No. 08/400,397 filed Mar. 7, 1995 now abandoned, which is Continuation-In-Part of U.S. Ser. No. 08/382,958 filed Feb. 2, 1995, now abandoned, which is a continuation of U.S. Ser. No. 08/082,291 filed Jun. 24, 1993, now abandoned.

Please replace the paragraph from page 17, line 9 to page 17, line 12 with the following rewritten paragraph:

Figures. ~~3a(1), 3a(2), 3b(1) and 3b(2)~~ 3A-1, 3A-2, 3B-1 and 3B-2 illustrate the control of data transfer between stages of a preferred embodiment of a pipeline using a two-wire interface and a multi-phase clock;

Please replace pages 36-50 of the specification with the enclosed pages 36-50.

Please replace pages 256-263 of the specification with the enclosed pages 256-263.

Please replace page 270 of the specification with the enclosed page 270.

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Please replace pages 290-293 of the specification with the enclosed pages 290-293.

Please replace pages 295-303 of the specification with the enclosed pages 295-303.

Please replace page 305 of the specification with the enclosed page 305.

Please replace pages 307-311 of the specification with the enclosed pages 307-311.

Please replace pages 316-321 of the specification with the enclosed pages 316-321.

Please replace pages 338 - 347 of the specification with the enclosed pages 338 - 347.

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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (ORIGINAL) An apparatus for decompressing video data, comprising:

a start code detector to convert a portion of a stream of video data into a stream of data tokens in response to detecting a start code sequence in said stream of video data; and

a pipeline having stages and being capable of decoding video data , the start code detector being coupled to send the data tokens to the pipeline.

2. (CURRENTLY AMENDED) The apparatus of claim 1, wherein a plurality of the stages of said pipeline have operating modes responsive to [the] a format of said tokens.

3. (ORIGINAL) The apparatus of claim 1, further comprising an inserter of search mode tokens to transmit search mode tokens into the stream of video data.

4. (ORIGINAL) The apparatus of claim 1, wherein the start code detector is capable of searching for video start codes complying with different formats.

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5. (ORIGINAL) The apparatus of claim 4, wherein said formats include formats complying with at least two of the video standards selected from the group consisting of JPEG, MPEG, and H.261.

6. (ORIGINAL) The apparatus of claim 3, wherein the start code detector ignores video data until a video start code is found in response to receiving one of the search mode tokens.

7. (ORIGINAL) The apparatus of claim 1, further comprising:
two-wire interfaces coupling the consecutive stages of the pipeline.

8. (ORIGINAL)The apparatus of claim 7, wherein the two-wire interfaces transmit data valid and data acceptance signals.

9. (ORIGINAL) The apparatus of claim 1, wherein the start code detector is adapted to introduce new tokens into the stream of video data at detected start code sequences.

10. (ORIGINAL) The apparatus of claim 2, wherein a portion of the stages of the pipeline reconfigure themselves to process data in response to receiving predetermined types of tokens.

11. (ORIGINAL) The apparatus of claim 9, wherein the start code detector introduces picture end tokens into the stream of video data.

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12. (ORIGINAL) The apparatus of claim 1, wherein the start code detector is a hardware device.

13. (ORIGINAL) The apparatus of claim 1, wherein the pipeline includes:

a Huffman decoder coupled to receive data from the start code detector;

a token formatter coupled to data from the Huffman decoder;

an inverse modeler coupled to receive data from the token formatter; and

an inverse quantizer coupled to receive data from the inverse modeler.

14. (ORIGINAL) A method for decoding encoded video data, comprising:

receiving a portion of a video data stream in a multi-stage pipelined decoder;

inserting tokens into the received portion of the video data stream at least one of the tokens being a search mode token;

detecting the search mode token in a special one of the stages; and

searching for a start code token in the video data stream in response to detecting the search mode token in the special one of the stages.

15. (ORIGINAL) The method of claim 14, further comprising:

making a random access into the data stream to receive the portion of the video stream; and

wherein the search mode token is inserted in response to making the random access.

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16. (ORIGINAL) The method of claim 15, wherein the random access results from one of an error and a channel switch.

17. (ORIGINAL) The method of claim 15, further comprising:

reconfiguring stages of the decoder to decode video data in response to detecting the start code token.

18. (ORIGINAL) The method of claim 17, wherein searching recognizes start code tokens corresponding to video data encoded according to one of the standards MPEG, JPEG, and H.261.

19. (ORIGINAL) A pipelined decoder for processing encoded video data, comprising:

a pipeline having a plurality of stages for receiving and decoding a portion of a video data stream;

a means for inserting tokens into the video data stream at least one of the tokens being a search mode token; and

a start code detector to search for start code tokens in the video data stream in response to detecting the search mode token.

20. (ORIGINAL) The decoder of claim 19, wherein the means for inserting inserts a search mode token into the data stream in response to making a random access into the video data stream.

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21. (ORIGINAL) The decoder of claim 20, wherein the random access results from one of an error and a channel switch.

22. (ORIGINAL) The decoder of claim 20, wherein a plurality of the stages reconfigure themselves to decode video data in response a start code token.

23. (ORIGINAL) The decoder of claim 22, wherein the start code token corresponds to video data encoded according to one of the standards MPEG, JPEG, and H.261.

24. (ORIGINAL) The decoder of claim 20, further comprising:

a semiconductor substrate, the pipeline, means for inserting and start code detector being located on the substrate.

25. (ORIGINAL) A system for decoding video data into picture frames, comprising:

a start code detector to search for a start code sequence in a stream of video data in response to detecting a search mode token therein and to convert a portion of the stream of video data into data tokens in response to detecting a start code sequence in said stream of video data; and

a decoder coupled to receive the data tokens from the start code detector and to decode the received data tokens into picture frames, the decoder capable of decoding multiple standards.

26. (ORIGINAL) The system of claim 25, further comprising an inserter of search mode tokens coupled to insert search mode tokens into the stream of video data.

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27. (ORIGINAL)The system of claim 25, wherein the standards include two of JPEG, MPEG, and H.261.

28. (ORIGINAL) The system of claim 25, wherein the decoder further comprises:

a Huffman decoder;

an inverse quantizer coupled to the Huffman decoder; and

an inverse discrete cosine transformer coupled to the inverse quantizer.

29. (ORIGINAL) The system of claim 25, wherein the decoder is a hardware device.

REMARKS

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I. Status

In the Office Action mailed June 30, 2003, the Examiner noted that claims 1-29 were pending and rejected claims 1-29. Claim 2 has been amended, Thus, in view of the foregoing, claims 1-29 remain pending for reconsideration, which is requested. No new matter has been added. The applicant respectfully traverses the rejection.

II. Oath/Declaration

The applicant respectfully requests that the applicant be permitted to submit a supplemental declaration after allowance which will also include the correction noted by the Examiner.

III. Specification

The informalities objected to have been corrected, except for the page numbers 16a-16l and pages 24a, 24b. The CFR and MPEP, particularly the relevant sections 37 CFR 1.71 and MPEP 608.01 do not specify a numerical system for numbering pages. Since the sequence of the specification is clear from the present numbering system, and changing it now would result in significant expense and confusion, the Applicant requests that this objection be dropped.

The Examiner requested detailed support for claims 1-10. FIGs 11, 12, and 13 illustrate an overview of one possible example of the apparatus and method of claims 1-10. A display mechanism is shown in FIG. 13. Components of the decoding process are illustrate in FIG. 11. Support for tokens starts on page 51, and on page 104, line 23 to page 108, line 29. Support for the "formatter" is on page 134, line 9 to page 135, line 27.

Further information of the structure and operation of the invention of claims 1-11 is given in an illustrative embodiment of the invention which is set

for in sections 1-27 (see page 84, line 30 to page 85, line 22). Components of the decoding process are illustrated, such as the Inverse Modeler 23 (page 146, lines 20-31), Inverse Quantizer 24 (page 146, line 33 to page 147, line 28), Huffman Decoder and Parser 25 (page 147, line 19 to page 151, line 12), and Diverse Discrete Cosine Transformer 26 (page 151, line 13 to page 152, line 5).

Figure 20 shows an embodiment of a Start Code Detector. Figure 21 illustrates a start code in a data stream. The Start-Code Detector is described from page 113, line 19 to page 120, line 28. FIGs 20 and 21 are explained in the specification from page 78, line 32 to page 80, line 22.

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IV. Information Disclosure Statement

The documents requested by the Examiner are enclosed herein.

V. Double Patenting

The Applicants submits a Terminal Disclaimer for the purpose of overcoming the double patenting rejection of U.S. Patent 5,978,592. However, Applicants do not admit to any characterization or limitation of the claims by the Examiner, particularly any that are inconsistent with the language of the claims considered in their entirety and including all of their constituent limitations.

VI. Rejection of claims under 35 U.S.C. § 112, second paragraph

In claim 1, "the data tokens" (line 6) properly refers back to "data tokens" (line 3). In claim 7, "the consecutive stages" properly refers back to "stages" (claim 1, line 5) which are consecutive. Claim 2 has been amended to clarify the relationship of "format". The claims being in proper form, the Applicant requests that the Examiner drop this rejection.

VII. Rejection of claims under 35 U.S.C. § 102

Claims 1-5, 7, 8, 10, 12-15, 17-20, 22-24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gonzales et al.

The Start Code Detector of the present invention is capable of taking bit

streams of different formats (e.g. MPEG, JPEG, H.261) and generating from them a sequence of proprietary tokens which are meaningful to the rest of the decoder.

To support the allegation that Gonzales et al. discloses a start code detector to convert a portion of a stream of video data into a stream of data tokens in response to detecting a start code sequence in the stream of video data, the Office Action cites to Figure 3A, column 8, lines 47-67, and column 10, line 61-column 11, line 5 of Gonzales et al. However, the Applicant respectfully submits that these sections do not disclose a start code detector. For example, Fig 3A merely shows a buffer with blocks of data separated by end-of-block marks. Similarly, column 8, lines 47-67 describes blocks of data with header information and end-of-block markers. Column 10, line 61- column 11, line 5 discloses Run Length Coded image data. In summary, none of these sections disclose a start code detector converting a portion of a stream of video data into a stream of data tokens in response to detecting a start code sequence in the stream of video data. In particular, the elements of "start code detector", "data tokens" and "start code sequence" is missing from the disclosure.

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Furthermore, the cited prior art does not disclose "data tokens" or "tokens" as cited in claims 1-29. A "token" of the present invention is defined in the specification as "interactive interfacing messenger package for control and /or data functions." (page 24b, lines 11-13). This entails a technology more powerful than a traditional token, for example, in the context of token rings, or a traditional packet of information. Gonzales et al. does not disclose this technology.

As for claim 2, to support the allegation that Gonzales et al. discloses pipeline stages having operating modes responsive to the format of a token, the Office Action cites to column 13, lines 1-26 of Gonzales et al. This section appears to disclose data movement to and from a byte buffer, but does not disclose a "token" or a stage having an "operating mode" responsive to the format of the token.

As for claim 3, to support the allegation that Gonzales et al. discloses an

inserter of search mode tokens to transmit search mode tokens into the stream of data, the Office Action has cited to column 11, lines 25-41. However, this cited section discloses bits which indicate quantization, resets internal DE predictors, and resets an internal DC predictor. These functions are unrelated to a search mode token as recited in claim 3.

As for claim 4, column 9, line 40 to column 10, line 11 of Gonzales et al. discloses a JPEG compression/decompression algorithm, and does not disclose "searching for video start codes" as recited in claim 4.

As for claim 8, column 5, lines 5-50 of Gonzales et al. discloses two buffers 16a and 16b between two stages of a pipeline, and does not disclose a "two-wire interface" which transmits "data valid and data acceptance signals".

As for claim 10, column 12, lines 4-15 discloses a processing cycle of a DCT phase, and does not show stages of the pipeline "reconfiguring" themselves in response to tokens as recited in claim 10.

As for claim 12, column 9, lines 55-59 of Gonzales et al. does not disclose a "start code detector" in a hardware device.

As for claim 13, the prior art does not disclose a "start code detector", a "token formatter", or an "inverse modeler". Figure 5 discloses a decoding process, but does not disclose a "token formatter" or a "start code detector".

As for claim 14, the cited prior art does not disclose "tokens" (line 3), at least one of the tokens being a "search mode token" (line 4), "detecting the search mode token" in one of the stages (line 5), and "searching for a start code token in the video data stream" (line 6). As discussed above in the applicant's traverse to claims 1-4, the cited sections of the prior art do not show these features.

As for claim 19, the cited prior art does not disclose "tokens" (line 4), at least one of the tokens being a "search mode token" (line 5), and "a start code detector to search for start code tokens in the video data stream" (line 6). As discussed above, the cited sections of the prior art do not show these features.

As for claim 25, the cited prior art does not disclose "a start code detector to search for a start code sequence in a stream of video data" (lines 2-

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3) and a decoder capable of decoding multiple standards (line 7-8). As discussed above, the cited sections of the prior art do not show these features.

Therefore, the present invention recited in claims 1-29 is not rendered obvious by the cited prior art.

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VIII. Rejection of claims under 35 U.S.C. § 103(a)

Claims 6, 9, 11, 16, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gonzales et al. in view of Normile et al.

The Examiner concedes that Gonzales et al. does not disclose the start code detector ignoring video data until a video start code is found in response to receiving one of the search mode tokens. However, the Office Action alleges that Normile et al. discloses this feature in column 13, line 47-column 14, line 9 and column 16, lines 29-32. However, the recited sections of Normile et al. disclose a method for encoding motion video as shown in Fig 7(a). In contrast, the present invention decodes and decompresses data. Furthermore, the cited sections do not show "a start code detector" nor "search mode tokens".

Furthermore, Normile et al. does not disclose a "start detector", "tokens", nor a search mode.

Thus, neither of the references Gonzales et al. nor Normile et al. separately, or in combination, have disclosed the above features of claims 6, 9, 11, 16 and 21.

Therefore, the present invention recited in claims 1-29 is not rendered obvious by the cited prior art.

IX. Concluding Matters

In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims distinguishes over the prior art, and therefore, defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowance of all the pending claims is respectfully requested.

Should there be any remaining questions to correct format matters, it is urged that the Examiner contact the undersigned attorney with a telephone interview to expedite and complete prosecution.

If any further fees are required in connection with the filing of this response, please change same to our Deposit Account No. 04-1175.

Respectfully submitted,

DISCOVISION ASSOCIATES

Date: September 24, 2003

Richard J. Stokey
Reg. No. 40,383

DISCOVISION ASSOCIATES
INTELLECTUAL PROPERTY DEVELOPMENT
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Abstract

An apparatus and method for compressing video data comprises a start code detector to convert a portion of a stream of video data into a stream of data tokens in response to detecting a start code sequence in the stream of video data and a pipeline having stages and being capable of decoding video data. The start code detector sends the data tokens to the pipeline.

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SUPPLEMENTAL DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

Attorney Docket Numb	004(EP)USC1X PDDD
First Named Inventor	ADRIAN P. WISE
COMPLETE IF KNOWN	
Application Number	08/400,397
Filing Date	MARCH 7, 1995
Group Art Unit	2302
Examiner Name	J. HARRITY

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled :

DATA PIPELINE SYSTEM AND DATA ENCODING METHOD WITH START CODE DETECTOR

(Title of the Invention)

the specification of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) 03/07/1995 as United States Application Number or PCT International Application Number 08/400,397 and was amended on (MM/DD/YYYY) 06/11/1997 (if applicable). 11/18/1996; 02/24/1997;

I hereby declare that the subject matter of the ☐ attached amendment ☐ amendment filed on _____ was part of my or our invention and was invented before the filing date of the original application, above identified for such invention.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365 (a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	Certified Copy Attached? NO
92306038.8	EPO	06/30/1992	☐	☐	☒
9405914.4	GREAT BRITAIN	03/24/1994	☐	☐	☒
9504019.2	GREAT BRITAIN	02/28/1995	☐	☐	☒
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority sheet attached hereto:

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	
		☐ Additional provisional application numbers are listed on a supplemental priority sheet attached hereto.

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks, Washington, DC 20231.

Type a plus sig[illegible]de this box → [+]

PTO/SB/64 (8-95)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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DECLARATION

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)
08/082,291		06/24/1993	
08/382,952		02/01/1995	5,519,339

COPY

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority sheet attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Name	Registration Number	Name	Registration Number
Ronald J. Clark	21,058		
Robert T. Braun	36,758		
Arthur S. Bickel	34,123		

☐ Additional registered practitioner(s) named on a supplemental sheet attached hereto.

Direct all correspondence to:

Name	Robert T. Braun				
Address	2355 Main Street, Suite 200				
Address					
City	Irvine	State	CA	ZIP	92614
Country	USA	Telephone	(714) 660-5000	Fax	(714) 660-1801

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name	ADRIAN	Middle Initial	P	Family Name	WISE	Suffix e.g. Jr.	

Inventor's Signature: A P Wise Date: 17 July 97

Residence: City	BRACKNELL, BERKS	State		Country	UNITED KINGDOM	Citizenship	UK
Post Office Address	17 ALBEN ROAD						
Post Office Address	BINFIELD						
City	BRACKNELL	State		Zip	RG42 4HU	Country	UNITED KINGDOM

☒ Additional inventors are being named on supplemental sheet(s) attached hereto

Type a plus si[illegible] ide this box → [+]

PTO/SB/04 (8-96)
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DECLARATION

ADDITIONAL INVENTOR(S) Supplemental Sheet

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
MARTIN	W	SOTHERAN	

Inventor's Signature: M. Sotheran Date: 7th July '97.

Residence: City BRISTOL State Country UNITED KINGDOM Citizenship UK

Post Office Address: 24 HOME FARM WAY

Post Office Address: EASTER COMPTON

City BRISTOL State Zip BS12 3SE Country UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
WILLIAM	P	ROBBINS	

Inventor's Signature: Date:

Residence: City BRISTOL State Country UNITED KINGDOM Citizenship UK

Post Office Address: 2 WINDSOR TERRACE

Post Office Address: CLIFTON

City BRISTOL State Zip BS8 4LW Country UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
ANTHONY	M	JONES	

Inventor's Signature: Date:

Residence: City NIJMEGEN State Country NETHERLANDS Citizenship UK

Post Office Address: NIJMEEGSEBAAN 45 CB NIJMEGEN

Post Office Address: HEILIG LAND STICHTING

City NIJMEGEN State Zip 6564 Country UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
HELEN	R	FINCH	

Inventor's Signature: Date:

Residence: City BRISTOL State Country UNITED KINGDOM Citizenship UK

Post Office Address: 41 DRUID WOODS - AVON WAY

Post Office Address:

City BRISTOL State Zip BS9 1SZ Country UNITED KINGDOM

☒ Additional inventors are being named on supplemental sheet(s) attached hereto

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DECLARATION

ADDITIONAL INVENTOR(S) Supplemental Sheet

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
MARTIN	W	SOTHERAN	

Inventor's Signature: | Date:

Residence: City	State	Country	Citizenship
BRISTOL		UNITED KINGDOM	UK

Post Office Address: 24 HOME FARM WAY

Post Office Address: EASTER COMPTON

City	State	Zip	Country
BRISTOL		BS12 3SE	UNITED KINGDOM

COPY

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
WILLIAM	P	ROBBINS	

Inventor's Signature: [signature] | Date: 8 July 97

Residence: City	State	Country	Citizenship
BRISTOL		UNITED KINGDOM	UK

Post Office Address: 2 WINDSOR TERRACE

Post Office Address: CLIFTON

City	State	Zip	Country
BRISTOL		BS8 4LW	UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
ANTHONY	M	JONES	

Inventor's Signature: | Date:

Residence: City	State	Country	Citizenship
NIJMEGEN		NETHERLANDS	UK

Post Office Address: NIJMEEGSEBAAN 45 CB NIJMEGEN

Post Office Address: HEILIG LAND STICHTING

City	State	Zip	Country
NIJMEGEN		6564	UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
HELEN	R	FINCH	

Inventor's Signature: | Date:

Residence: City	State	Country	Citizenship
BRISTOL		UNITED KINGDOM	UK

Post Office Address: 41 DRUID WOODS - AVON WAY

Post Office Address:

City	State	Zip	Country
BRISTOL		BS9 1SZ	UNITED KINGDOM

☒ Additional inventors are being named on supplemental sheet(s) attached hereto

Type a plus sign (+) inside this box → [+]

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Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
MARTIN	W	SOTHERAN	

Inventor's Signature: | Date:

Residence: City BRISTOL | State | Country UNITED KINGDOM | Citizenship UK

Post Office Address: 24 HOME FARM WAY

Post Office Address: EASTER COMPTON

City BRISTOL | State | Zip BS12 3SE | Country UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
WILLIAM	P	ROBBINS	

Inventor's Signature: | Date:

Residence: City BRISTOL | State | Country UNITED KINGDOM | Citizenship UK

Post Office Address: 2 WINDSOR TERRACE

Post Office Address: CLIFTON

City BRISTOL | State | Zip BS8 4LW | Country UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
ANTHONY	M	JONES	

Inventor's Signature: AMJones | Date: May 28, 1998

Residence: City ARNHEM-ZUID | State | Country NETHERLANDS | Citizenship UK

Post Office Address: MUNTENDAMPAD 1

Post Office Address: 6835 BE ARNHEM-ZUID

City ARNHEM-ZUID | State | Zip 6835 | Country NETHERLNADS

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
HELEN	R	FINCH	

Inventor's Signature: | Date:

Residence: City BRISTOL | State | Country UNITED KINGDOM | Citizenship UK

Post Office Address: 41 DRUID WOODS - AVON WAY

Post Office Address:

City BRISTOL | State | Zip BS9 1SZ | Country UNITED KINGDOM

☒ Additional inventors are being named on supplemental sheet(s) attached hereto

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Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
MARTIN	W	SOTHERAN	

Inventor's Signature: Date:

Residence: City BRISTOL State: Country UNITED KINGDOM Citizenship UK

Post Office Address: 24 HOME FARM WAY

Post Office Address: EASTER COMPTON

City BRISTOL State: Zip BS12 3SE Country UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
WILLIAM	P	ROBBINS	

Inventor's Signature: Date:

Residence: City BRISTOL State: Country UNITED KINGDOM Citizenship UK

Post Office Address: 2 WINDSOR TERRACE

Post Office Address: CLIFTON

City BRISTOL State: Zip BS8 4LW Country UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
ANTHONY	M	JONES	

Inventor's Signature: Date:

Residence: City NIJMEGEN State: Country NETHERLANDS Citizenship UK

Post Office Address: NIJMEEGSEBAAN 45 CB NIJMEGEN

Post Office Address: HEILIG LAND STICHTING

City NIJMEGEN State: Zip 6564 Country UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
HELEN	R	FINCH	

Inventor's Signature: [signature] Date: 11th July 1997

Residence: City BRISTOL State: Country UNITED KINGDOM Citizenship UK

Post Office Address: 41 DRUID WOODS - AVON WAY

Post Office Address:

City BRISTOL State: Zip BS9 1SZ Country UNITED KINGDOM

☒ Additional inventors are being named on supplemental sheet(s) attached hereto

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DECLARATION

ADDITIONAL INVENTOR(S) Supplemental Sheet

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
KEVIN	J	BOYD	

Inventor's Signature: [signature] Date: 4/7/97

Residence: City: BRISTOL State: Country: UNITED KINGDOM Citizenship: UK

Post Office Address: 21 LANCASHIRE ROAD

Post Office Address:

City: BRISTOL State: Zip: BS7 9DL Country: UNITED KINGDOM

COPY

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
ANTHONY PETER	J	CLAYDON	

Inventor's Signature: Date:

Residence: City: BATH AVON State: Country: UNITED KINGDOM Citizenship: UK

Post Office Address: 14 SYDNEY BUILDINGS

Post Office Address:

City: BATH AVON State: Zip: BA2 6BZ Country: UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.

Inventor's Signature: Date:

Residence: City: State: Country: Citizenship:

Post Office Address:

Post Office Address:

City: State: Zip: Country:

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.

Inventor's Signature: Date:

Residence: City: State: Country: Citizenship:

Post Office Address:

Post Office Address:

City: State: Zip: Country:

☐ Additional inventors are being named on supplemental sheet(s) attached hereto

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DECLARATION

ADDITIONAL INVENTOR(S) Supplemental Sheet

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	KEVIN	Middle Initial	J	Family Name	BOYD	Suffix e.g. Jr.	

Inventor's Signature: | Date:

Residence: City	BRISTOL	State		Country	UNITED KINGDOM	Citizenship	UK

Post Office Address: 21 LANCASHIRE ROAD

Post Office Address:

City	BRISTOL	State		Zip	BS7 9DL	Country	UNITED KINGDOM

COPY

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	ANTHONY PETER	Middle Initial	J	Family Name	CLAYDON	Suffix e.g. Jr.	

Inventor's Signature: [signature] | Date:

Residence: City	BATH AVON	State		Country	UNITED KINGDOM	Citizenship	UK

Post Office Address: 14 SYDNEY BUILDINGS

Post Office Address:

City	BATH AVON	State		Zip	BA2 6BZ	Country	UNITED KINGDOM

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name		Middle Initial		Family Name		Suffix e.g. Jr.	

Inventor's Signature: | Date:

Residence: City		State		Country		Citizenship	

Post Office Address:

Post Office Address:

City		State		Zip		Country	

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name		Middle Initial		Family Name		Suffix e.g. Jr.	

Inventor's Signature: | Date:

Residence: City		State		Country		Citizenship	

Post Office Address:

Post Office Address:

City		State		Zip		Country	

☐ Additional inventors are being named on supplemental sheet(s) attached hereto

PTO/SB/26 (05-03)
Approved for use through 4/30/2003. OMB 0651-0031
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A PRIOR PATENT	Docket Number (Optional) 94100412(EP)USC1X1C1D1PDDD

In re Application of: Wise et al.

Application No.: 09/770,157

Filed: 1/26/2001

For: MULTISTANDARD VIDEO DECODER AND DECOMPRESSION SYSTEM FOR PROCESSING...THERETO

The owner*, Discovision Associates, of 100 percent interest in the instant application hereby **disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. 154 and 173, as presently shortened by any terminal disclaimer, of prior Patent No. 5,978,592 The owner hereby agrees that any patent** so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the prior patent, as presently shortened by any terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ **For submissions on behalf of an organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the organization.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ **The undersigned is an attorney or agent of record.**

Signature — Date: Sept. 24, 2003

Richard J. Stokey, Reg. No. 40,383
Typed or printed name

(949) 660-5006
Telephone Number

☒ **Terminal disclaimer fee under 37 CFR 1.20(d) included.**

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

• Statement under 37 CIFIR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Adrian P. Wise	§	Application No.: Not Yet Known
Filed: HEREWITH	§	Art Unit: 2783 (anticipated)
For: MULTISTANDARD VIDEO DECODER AND DECOMPRESSION SYSTEM FOR PROCESSING ENCODED BIT STREAMS INCLUDING START CODE DETECTION AND METHODS RELATING THERETO	§	Examiner: Follansbee, J. (anticipated)

COPY

DUPLICATE

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97

BOX PATENT APPLICATION
Assistant Commissioner of Patents
Washington DC 20231

FILING OF CORRESPONDENCE BY EXPRESS MAIL UNDER 37 C.F.R. § 1.10

TB628505295US (*Express Mail Label* Number) — 1/26/01 (Date of Deposit)

Sir:

In complying with the duty of disclosure set forth in 37 CFR § 1.56, Applicant submits lists of patents and publications (these were previously submitted in 09/307,239) as listed on the attached form PTO-1449, and a concise explanation of the relevance of each listed item not in the English language as follows:

No non-English language references are submitted.

The Commissioner is hereby authorized to charge payment of the fee required by 37 C.F.R. § 1.17(i), 37 C.F.R. § 1.17(p), and any fees associated with this communication or credit any overpayment to Deposit Account No. 04-1175.

Respectfully submitted,

Date: 1/25/01

DISCOVISION ASSOCIATES

DISCOVISION ASSOCIATES
INTELLECTUAL PROPERTY DEVELOPMENT
P.O. Box 19616
Irvine, California 92623
(949) 660-5006

Richard Stokey
Reg. No. 40,383

RS:sd

Form PTO-1449 (Modified)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

37 CFR 1.98(b))

MAIL ROOM
FEB 27 1997
PAT. & TRADEMARK OFF.

DUPLICATE

ATTY. DOCKET NO.	SERIAL NO.
941004(EP)USC1X	~~400387~~ 09/807239
APPLICANT: ADRIAN P. WISE ET AL	
FILING DATE: MARCH 7, 1996	GROUP: ~~2302~~ 2753

COPY

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	AA	3875391	04/01/75	SHAPIRO ET AL	235	156	11/02/73
JH	AB	4225920	09/30/80	STOKES	364	200	09/11/78
JH	AC	4228497	10/14/80	GUPTA ET AL	364	200	11/17/77
JH	AD	4307447	12/22/81	PROVANZANO ET AL	364	200	06/19/79
JH	AE	4467409	08/21/84	POTASH ET AL	364	200	08/05/80
JH	AF	4617657	10/14/86	DRYNAN ET AL	370	60	12/31/84
JH	AG	4710866	12/01/87	ZOLNOWSKY ET AL	364	200	10/07/86
JH	AH	4809159	02/28/89	SOWA	364	200	01/21/88
JH	AI	4811214	03/07/89	NOSENCHUCK ET AL	364	200	11/14/86
JH	AJ	4811413	03/07/89	KIMMEL	382	41	10/22/87
JH	AK	4841436	06/20/89	ASANO ET AL	364	200	05/30/86
JH	AL	4855947	08/08/89	ZAREMBOWSKI ET AL	364	200	05/27/87
JH	AM	4922413	05/01/90	DOLECEK	364	200	01/15/83
JH	AN	4953082	08/28/90	NOMURA ET AL	364	200	02/15/89
JH	AO	4989138	01/29/91	RADOCHONSKI	364	200	05/14/90
JH	AP	5043880	08/27/91	YOSHIDA	364	200	01/23/89
JH	AQ	5184347	02/02/93	Farwell et al.	370	94.1	07/09/91
JH	AR	5203003	04/13/93	DONNER	395	800	03/23/91
JH	AS	5218436	06/08/93	SUGIYAMA ET AL	358	141	01/23/91
JH	AT	5227863	07/13/93	Bilbrey et al.	348	573	08/07/90
JH	AU	5297263	03/22/94	OHTSUKA ET AL	395	375	04/17/92
JH	AV	5301344	04/05/94	KOLCHINSKY	395	800	01/29/91

EXAMINER	DATE CONSIDERED
John Harvey	5/27/97

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO. 941004(EP)USC1X

SERIAL NO. ~~438397~~ 09/307239

APPLICANT
ADRIAN P. WISE ET AL

FILING DATE
MARCH 7, 1995

GROUP ~~2200~~ 2783

MAIL ROOM
FEB 27 1997
PAT. & TRADEMARK OFF.

37 CFR 1.98(b))

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EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	AW	5309563	05/03/94	FARRAND ET AL	395	200	09/09/91
JH	AX	5329313	07/12/94	KEITH	348	422	10/01/93
JH	AY	5329613	07/12/94	PAGE ET AL	395	200	10/30/92
JH	AZ	5333212	07/26/94	LIGTENBERG	382	56	11/17/92
JH	BA	5333266	07/26/94	BOAZ ET AL	395	200	03/27/92
JH	BB	5341371	08/23/94	SIMPSON	370	85.4	05/24/91
JH	BC	5406279	04/11/95	ANDERSON ET AL	341	51	09/02/92
JH	BD	5414813	05/09/95	SHIOBARA	395	200	11/01/93
JH	BE	5442790	08/15/95	NOSENCHUCK	395	700	03/09/94
JH	BF	5446866	08/29/95	DRAKO ET AL	395	500	01/30/92
JH	BG	5450599	09/12/95	HORVATH ET AL	395	800	06/04/92
JH	BH	5452006	09/19/95	AULD	348	390	10/25/93
JH	BI	5461679	10/24/95	NORMILE ET AL	395	650	05/14/93
JH	BJ	5481689	01/02/96	STAMM ET AL	395	412	08/13/93
JH	BK	5487064	01/23/96	GALAND ET AL	370	60	05/31/94
JH	BL	5490247	02/06/96	TUNG ET AL	395	162	11/24/93
JH	BM	5497498	03/05/96	TAYLOR	395	800	09/29/93
JH	BN	5504869	04/02/96	UCHIDA	395	375	07/15/94
JH	BO	5535290	07/09/96	Allen	382	250	09/11/95
JH	BP	5566089	10/15/96	HOOGENBOOM	364	514A	10/26/94
JH	BQ	5579052	11/26/96	Artieri	348	416	05/24/94

EXAMINER: John Hanley

DATE CONSIDERED: 5/27/97

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Form PTO-1449 (Modified) | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTY. DOCKET NO. PDCC P94:004(EP)USC1CIP | SERIAL NO. ~~08/~~ 08/430,239

INFORMATION DISCLOSURE STATEMENT BY APPLICANT | APPLICANT Wise et al.

(Use several sheets if necessary) | FILING DATE 03/07/95 | GROUP ~~2307~~ ~~2308~~ 2783

37 CFR 1.98(b)

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	AA	3 3 9 3 0 4 2	7/1/75	Whitman et al.	331	55	12/12/73
previously filed	~~AB~~	~~3 9 5 2 5 3 5~~	~~6/8/76~~	~~Belle Isle~~	~~340~~	~~172.5~~	~~3/3/74~~
JH	AC	4 1 0 7 7 3 0	8/15/78	Grimsdale et al.	364	521	1/25/77
JH	AD	4 1 4 2 2 0 5	2/27/79	Iinuma	358	13	7/13/77

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
JH	AE ✓	0 1 9 6 9 1 1	08.10.86	EP				
JH	AF ✓	0 2 5 5 7 6 7	10.02.88	EP				
JH	AG ✓	0 4 6 8 4 8 0	29.01.92	EP				

OTHER DOCUMENTS (Including Author, Title, Date**, Relevant Pages, Place of Publication***)

previously cited	~~AH~~	~~Chong, "A Data Flow Architecture For Digital Image Processing," WescomTech. Papers No. 1/3, 10/30/84, Anaheim, California, USA, pp. 1-10~~
JH	AI ✓	P. Yip, et al., "DIT and DIF Algorithm for Discrete Sine and Cosine Transforms" Proceedings of the International Symposium on Circuits and Systems, IEEE Press, New York, US, Vol. 2/3, 5 June 1985, Kyoto, JP, pages 941-944
JH	AJ ✓	Hsieh S. Hou, "A Fast Recursive Algorithm for Computing the Discrete Cosine Transform," IEEE Transactions on Acoustics, Speech, and Signal Processing, Vol. 35, No. 10, October 1987, IEEE Press, New York, US, pages 1455-1461
previously cited	~~AK~~	~~Komori et al., "An Elastic Pipeline Mechanism By Self Timed Circuits, IEEE Journal Of Solid State Circuits, Vol. 23, No. 1, 2/88, New York, NY, USA, pp. 111-117~~
JH	AL ✓	A. Gupta et al., "A Fast Recursive Algorithm for the Discrete Sine Transform," IEEE Transactions on Acoustics, Speech, and Signal Processing, Vol. 38, No. 3, March 1990, IEEE Press, New York, US, pages 553-557
JH	AM ✓	H.R. Wu, et al., "A Two Dimensional Fast Cosine Transform Algorithm Based on Hou's Approach," IEEE Transaction on Acoustics, Speech, and Signal Processing, Vol. 39, No. 2, February 1991, IEEE Press, New York, US, pages 544-546

EXAMINER John Hamilton | DATE CONSIDERED 11/21/96

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Form PTO-1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. POCO P94:004EPIUSC1CIP	SERIAL NO. ~~08/xxx,xxx~~ 09/357,835
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) COPY	APPLICANT Wisa et al.	
(37 CFR 1.98(b)		FILING DATE 03/07/95	GROUP ~~231~~ ~~233~~ 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
previously filed	~~AN~~	~~4 4 4 5 8 4 8~~	~~4/10/79~~	~~Fite~~	~~364~~	~~200~~	~~5/8/77~~
JH	AO	4 1 3 5 4 4 3	4/1/80	Whitehouse et al.	358	136	5/15/78
JH	AP	4 2 1 5 3 6 9	7/29/80	Iijima	358	146	12/15/78
JH	AQ	4 3 0 2 7 7 5	11/24/81	Widergren et al.	358	136	12/15/78
JH	AR	4 3 3 4 2 4 6	6/8/82	Saran	358	261	5/15/80
JH	AS	4 4 3 3 3 0 8	2/21/84	Hirata	331	17	12/3/81
JH	AT	4 4 3 7 0 7 2	3/13/84	Asami	331	1A	9/21/82
JH	AU	4 4 9 5 6 2 9	1/22/85	Zasio et al.	377	70	1/25/83
JH	AV	4 5 4 0 9 0 3	9/10/85	Cocke et al.	307	465	10/17/83

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
JH	AW ✓	0 5 7 2 2 6 2	01.12.93	EP				
JH	AX ✓	0 5 7 2 2 6 3	01.12.93	EP				
JH	AY ✓	0 5 7 6 7 4 9	05.01.94	EP				
JH	AZ ✓	0 5 8 9 7 3 4	30.03.94	EP			X	
JH	BA ✓	0 6 3 9 0 3 2	15.02.95	EP				
JH	BB ✓	2 0 4 5 0 3 5	22.10.80	GB				
JH	BC ✓	2 0 5 9 7 2 4	23.04.81	GB				
JH	BD ✓	2 1 7 1 5 7 8	28.08.86	GB				
JH	BE ✓	2 1 9 4 0 8 5	24.02.88	GB				

OTHER DOCUMENTS (Including Author, Title, Date**, Relevant Pages, Place of Publication***)

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	INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	APPLICANT Wright et al.	
(37 CFR 1.98(b)		FILING DATE 03/07/95	GROUP ~~2217~~ ~~2202~~ 2783

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	BI	4,563,006	4/1/86	Berndt	307	276	3/22/84
JH	BJ	4,630,136	12/16/86	I Yuan	364	200	2/21/84
JH	BK	4,644,151	2/24/87	Welles II et al.	358	149	2/1/85
JH	BL	4,679,103	7/7/87	Arnould et al.	364	725	3/8/85
JH	BM	4,747,070	5/24/88	Trottier et al.	364	900	1/9/84
JH	BN	4,785,349	11/15/88	Keith et al.	358	136	10/5/87
previously filed	~~BO~~	~~4,789,933~~	~~12/6/88~~	~~Hannan~~	~~364~~	~~200~~	~~4/7/86~~
JH	BP	4,799,779	1/24/89	Frederiksen	273	1E	2/24/86
previously filed	~~BQ~~	~~4,819,232~~	~~4/13/89~~	~~Simon et al.~~	~~359~~	~~133~~	~~11/13/87~~
JH	BR	4,829,540	5/9/89	Knauer et al.	364	725	6/19/86
JH	BS	4,831,633	5/16/89	Borgers et al.	358	133	3/24/88
JH	BT	4,868,866	9/12/89	Goodfellow et al.	358	13	9/30/88
previously filed	~~BU~~	~~4,868,868~~	~~9/12/89~~	~~Gonzalez Lopez et al~~	~~364~~	~~518~~	~~12/30/87~~
JH	BV	4,888,724	12/12/89	Okano et al.	364	518	8/24/87

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
JH	BW ✓	2,226,805	22.12.93	GB	—	—		
JH	BX ✓	2,269,074	26.01.94	GB	—	—		
	BY							
	BZ							

OTHER DOCUMENTS (Including Author, Title, Date**, Relevant Pages, Place of Publication***)

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ATTY. DOCKET NO.	SERIAL NO.
P000 P941004(EP\USC1CIP	~~08/[illegible]~~ 08/358,259
APPLICANT: Wise et al.	
FILING DATE: 03/07/95	GROUP: ~~2312~~ ~~2303~~ 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	CD	4,893,174	1/2/90	Kato et al.	364	900	1/9/88
JH	CE	4,903,013	2/20/90	Wiedach et al.	341	51	7/16/86
JH	CF	4,912,638	3/27/90	Aubie et al.	364	725	6/5/87
JH	CG	4,922,441	5/1/90	Strobach	358	136	9/26/88
JH	CH	4,928,242	5/8/90	Kitamura	358	12	9/15/88
JH	CI	4,928,243	5/8/90	Feuchtwanger	358	133	3/7/89
JH	CJ	4,975,955	12/4/90	Roberts et al.	307	272.2	7/20/88
JH	CK	4,991,112	2/5/91	Callemyn	364	518	12/21/88
JH	CL	5,003,465	3/26/91	Cushing et al.	307	465	12/19/89
JH	CM	5,027,271	6/25/91	Marlton et al.	358	183	12/6/89
JH	CN	5,038,296	8/6/91	Hang	358	136	8/6/91
JH	CO	5,053,985	10/1/91	Friedlander et al.	364	725	10/19/89
JH	CP	5,058,044	10/15/91	Cowley et al.	331	1A	10/29/90
JH	CQ	5,060,204	10/22/91	Arbeiter	375	122	2/24/89
JH	CR	5,081,626	1/14/92	Lucas et al.	340	728	3/9/90
JH	CS	5,086,426	2/4/92	Shimura	382	56	7/3/91

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	CT							
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	CW	
	CX	
	CY	

EXAMINER: JH

DATE CONSIDERED: 11/21/96

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ATTY. DOCKET NO.	SERIAL NO.
PDCO P941004(EP)USC1CIP	~~08/307,239~~ 08/317,239
APPLICANT: Wise et al.	
FILING DATE: 03/07/95	GROUP: ~~2317~~ ~~2303~~ 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	CZ	5,091,721	2/25/92	Hamori	340	727	12/22/88
JH	DA	5,101,435	4/21/92	Lee	358	432	5/29/91
JH	DB	5,111,292	5/5/92	Kuriacose et al.	358	133	2/27/91
JH	DC	5,113,256	5/12/92	Nagata et al.	358	136	5/11/90
JH	DD	5,122,873	6/16/92	Goiin	358	133	2/19/91
JH	DE	5,122,874	6/16/92	Raychaudhuri et al.	358	133	2/27/91
JH	DF	5,123,733	6/23/92	Nakayama	358	133	2/20/90
JH	DG	5,124,801	6/30/92	Andrews et al.	358	133	12/26/90
previously filed	~~DH~~	~~5,127,082~~	~~7/7/92~~	~~Hannah~~	~~395~~	~~136~~	~~1/23/91~~
JH	DI	5,130,563	7/14/92	Miller et al.	307	272.2	11/5/90
JH	DJ	5,134,487	7/28/92	Taguchi et al.	358	209	11/5/90
JH	DK	5,134,697	7/28/92	Scheffler	395	425	12/10/90
JH	DL	5,136,363	8/4/92	Savatier et al.	358	133	3/15/90
JH	DM	5,142,402	8/25/92	Sakagami et al.	358	432	10/18/90
JH	DN	5,142,405	9/8/92	Ng	358	135	4/29/91
JH	DO	5,142,406	9/8/92	Hasegawa	358	135	11/13/90

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	DP							
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EXAMINER	DATE CONSIDERED
John Hawley	11/21/96

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ATTY. DOCKET NO.	SERIAL NO.
P000 P941004/EP/USC1/CIP	~~08/307,239~~ 08/307239
APPLICANT: Wise et al.	
FILING DATE: 03/07/95	GROUP: ~~2307~~ ~~2300~~ 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	DV	5,141,321	9/15/92	Kato et al.	358	133	4/17/91
JH	DW	5,141,324	9/15/92	Harlin et al.	395	166	11/29/88
JH	DX	5,151,785	9/29/92	Sato	364	784	10/2/91
JH	DY	5,159,459	10/27/92	Allmendinger	358	136	12/26/91
JH	DZ	5,161,913	11/17/92	Music	358	13	4/3/91
JH	EA	5,168,366	12/1/92	Acampora et al.	358	133	12/20/91
JH	EB	5,168,368	12/1/92	Reisch et al.	358	432	9/18/91
JH	EC	5,170,272	12/15/92	Lauthold et al.	307	272.2	6/30/89
JH	ED	5,175,617	12/29/92	Wallace et al.	358	133	12/4/91
JH	EE	5,179,457	1/12/93	West et al.	340	799	3/29/91
JH	EF	5,181,118	1/26/93	Gersdorff et al.	358	133	4/19/91
JH	EG	5,181,184	2/2/93	Molpus et al.	341	50	1/2/91
JH	EH	5,185,693	2/9/93	Ng et al.	382	56	4/29/91
JH	EI	5,189,526	2/23/93	Sasson	358	432	9/21/90
JH	EJ	5,191,573	3/2/93	Balkanski et al.	364	725	1/3/92
JH	EK	5,198,933	3/9/93	Guichard et al.	358	133	3/25/91
JH	EL	5,201,056	4/6/93	Daniel et al.	395	800	5/2/90

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	EM							
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OTHER DOCUMENTS (Including Author, Title, Date**, Relevant Pages, Place of Publication***)

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EXAMINER	DATE CONSIDERED
John Hamilton	11/21/96

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ATTY. DOCKET NO.	SERIAL NO.
PCCD P94:004(EP)USC1CIP	~~08/~~ 09/307233
APPLICANT: Wise et al.	
FILING DATE: 03/07/95	GROUP: ~~2200~~ ~~2300~~ 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	ER	5,202,347	4/13/93	Bolton et al.	364	725	7/31/90
JH	ES	5,211,934	5/18/93	Ng et al.	353	135	8/16/92
JH	ET	5,211,927	5/18/93	Normile et al.	382	56	5/24/91
JH	EU	5,214,507	5/25/93	Aravind et al.	358	133	11/8/91
JH	EV	5,216,724	6/1/93	Suzuki et al.	382	7	8/23/92
JH	EW	5,222,205	6/29/93	Stone et al.	358	133	12/19/91
JH	EX	5,227,878	7/13/93	Puri et al.	358	136	11/15/91
JH	EY	5,227,879	7/13/93	Crinon et al.	382	56	6/14/91
JH	EZ	5,231,484	7/20/93	Kao et al.	353	426	12/24/90
JH	FA	5,231,486	7/27/93	Gonzales et al.	358	133	11/8/91
JH	FB	5,231,487	7/27/93	Acampora et al.	358	133	7/27/92
JH	FC	5,233,413	8/3/93	Piri et al.	358	149	4/10/85
JH	FD	5,233,414	8/3/93	Sherlock et al.	395	165	7/29/89
JH	FE	5,237,413	8/17/93	Israelsen et al.	358	160	11/19/91
JH	FF	5,241,382	8/31/93	Small et al.	307	449	12/20/91
JH	FG	5,241,383	8/31/93	Chen et al.	358	136	5/13/92

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	FH							
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OTHER DOCUMENTS (Including Author, Title, Date**, Relevant Pages, Place of Publication***)

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EXAMINER: John Hanley

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ATTY. DOCKET NO.	SERIAL NO.
POCO P94:CC4(EP)USC1C:P	~~08/307,000~~ 09/307,359
APPLICANT: Wise et al.	
FILING DATE: 03/07/95	GROUP: ~~2201~~ ~~2205~~ 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	HF	5,301,019	4/5/94	Citta	348	416	9/17/92
JH	HG	5,301,032	4/5/94	Hong et al.	358	261.2	12/4/92
JH	HH	5,301,040	4/5/94	Hoshi et al.	358	465	4/22/92
JH	HI	5,301,361	4/5/94	McMillan, Jr et al.	364	725	7/27/93
previously filed	~~HJ~~	~~5,301,362~~	~~4/5/94~~	~~Gonzales et al.~~	~~332~~	~~56~~	~~8/31/93~~
JH	HK	5,301,227	4/5/94	Atkins	395	165	11/25/92
JH	HL	5,303,242	4/12/94	Edge	395	164	12/22/92
JH	HM	5,303,353	4/19/94	Heim et al.	331	1A	6/1/93
JH	HN	5,305,438	4/19/94	MacKay et al.	395	164	5/19/92
JH	HO	5,303,382	5/3/94	Ohki	382	56	1/15/92
JH	HP	5,311,309	5/10/94	Ersoz et al.	348	409	5/30/91
JH	HQ	5,351,047	9/27/94	Behlen	341	67	9/21/92
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	HS						

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
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ATTY. DOCKET NO.	SERIAL NO.
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APPLICANT Wise et al.	
FILING DATE 3/7/95	**GROUP** ~~2308~~ 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH	AA	3 9 6 2 6 3 5	6/76	Belle-Isle	340	172.5	—
JH	AB	4 1 4 9 2 4 2	4/79	Pirz	364	200	—
JH	AC	4 7 8 9 9 2 7	12/88	Hannah	364	200	—
JH	AD	4 8 2 3 2 0 1	4/18/89	Simon et al.	358	133	—
JH	AE	4 8 6 6 6 3 7	9/12/89	Gonzalez-Lopez et al	364	518	—
JH	AF	5 1 2 9 0 5 9	7/7/92	Hannah	395	166	—
JH	AG	5 2 8 9 2 7 6	2/22/94	Siracusa et al.	348	467	—
JH	AH	5 2 8 9 5 7 7	2/22/94	Gonzales et al.	395	163	—
JH	AI	5 3 0 1 2 4 2	4/5/94	Gonzales et al.	382	56	—
	AJ						

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OTHER DOCUMENTS (Including Author, Title, Date**, Relevant Pages, Place of Publication***)

JH	AN ✓	Chong, "A Data Flow Architecture For Digital Image Processing," Wescon Tech. Papers No. 4/6, 10/30/84, Anaheim, California, USA, pp. 1-10
JH	AO ✓	Komori et al., "An Elastic Pipelline Mechanism By Self-Timed Circuits, IEEE Journal Of Solid-State Circuits, Vol. 23, No. 1, 2/88, New York, NY, USA, pp. 111-117
	AP	

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signals HIGH.

Comparing the state of the pipeline in Cycle 4 and Cycle 5, it can be seen that the provision of secondary storage elements, enables the pipeline embodiment shown in Fig. 2 to expand, that is, to free up data storage elements into which valid data can be advanced. For example, in Cycle 4, the data blocks D1, D2 and D3 form a "solid wall" since their data cannot be transferred until the ACCEPT signal into Stage F goes HIGH. Once this signal does become HIGH, however, data D1 is shifted out of the pipeline, data D2 is shifted into the primary storage elements of Stage F, and the secondary storage elements of Stage F become free to accept new data if the following device is not able to receive the data D2 and the pipeline must once again "compress". This is shown in Cycle 6, for which the data D3 has been shifted into the secondary storage elements of Stage F and the data D4 has been passed on from Stage D to Stage E as normal.

Figs. 3a(1), 3a(2), 3b(1) and 3b(2) (which are referred to collectively as Fig. 3) illustrate generally a preferred embodiment of the pipeline. This preferred embodiment implements the structure shown in Fig. 2 using a two-phase, non-overlapping clock with phases ø0 and ø1. Although a two-phase clock is preferred, it will be appreciated that it is also possible to drive the various embodiments of the invention using a clock with more than two phases.

As shown in Fig. 3, each pipeline stage is represented as having two separate boxes which illustrate the primary and secondary storage elements. Also, although the VALID signal and the data lines connect the various pipeline stages as before, for ease of illustration, only the ACCEPT signal is shown in Fig. 3. A change of state during a clock phase of certain of the ACCEPT signals is indicated in Fig. 3 using an upward-pointing arrow for changes from LOW to HIGH. Similarly, a downward-pointing arrow for changes from HIGH to

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LOW. Transfer of data from one storage element to another is indicated by a large open arrow. It is assumed that the VALID signal out of the primary or secondary storage elements of any given stage is HIGH whenever the storage elements contain valid data.

In Fig. 3, each cycle is shown as consisting of a full period of the non-overlapping clock phases ø0 and ø1. As is explained in greater detail below, data is transferred from the secondary storage elements (shown as the left box in each stage) to the primary storage elements (shown as the right box in each stage) during clock cycle ø1, whereas data is transferred from the primary storage elements of one stage to the secondary storage elements of the following stage during the clock cycle ø0. Fig. 3 also illustrates that the primary and secondary storage elements in each stage are further connected via an internal acceptance line to pass an ACCEPT signal in the same manner that the ACCEPT signal is passed from stage to stage. In this way, the secondary storage element will know when it can pass its date to the primary storage element.

Fig. 3 shows the ø1 phase of Cycle 1, in which data D1, D2 and D3, which were previously shifted into the secondary storage elements of Stages E, D, and B, respectively, are shifted into the primary storage elements of the respective stage. During the ø1 phase of Cycle 1, the pipeline, therefore, assumes the same configuration as is shown as Cycle 1 of FIG 2. As before, the ACCEPT signal into Stage F is assumed to be LOW. As Fig. 3 illustrates, however, this means that the ACCEPT signal into the primary storage element of Stage F is LOW, but
since this storage element does not contain valid data, it sets the ACCEPT signal into its secondary storage element HIGH.

The ACCEPT signal from the secondary storage elements of Stage F into the primary storage elements of Stage E is also

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set HIGH since the secondary storage elements of Stage F do not contain valid data. As before, since the primary storage elements of Stage F are able to accept data, data in all the upstream primary and secondary storage elements can be shifted downstream without any valid data being overwritten. The shift of data from one stage to the next takes place during the next ø0 phase in Cycle 2. For example, the valid data D1 contained in the primary storage element of Stage E is shifted into the secondary storage element of Stage F, the data D4 is shifted into the pipeline, that is, into the secondary storage element of Stage A, and so forth.

The primary storage element of Stage F still does not contain valid data during the ø0 phase in Cycle 2 and, therefore, the ACCEPT signal from the primary storage elements into the secondary storage elements of Stage F remains HIGH. During the ø0 phase in Cycle 2, data can therefore be shifted yet another step to the right, i.e., from the secondary to the primary storage elements within each stage.

However, once valid data is loaded into the primary storage elements of Stage F, if the ACCEPT into Stage F from the downstream device is still LOW, it is not possible to shift data out of the secondary storage element of Stage F without overwriting and destroying the valid data D1. The ACCEPT signal from the primary storage elements into the secondary storage elements of Stage F therefore goes LOW. Data D2, however, can still be shifted into the secondary storage of Stage F since it did not contain valid data and its ACCEPT signal out was HIGH.

During the ø1 phase of Cycle 3, it is not possible to shift data D2 into the primary storage elements of Stage F, although data can be shifted within all the previous stages. Once valid data is loaded into the secondary storage elements of Stage F, however, Stage F is not able to pass on this

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data. It signals this event setting its ACCEPT signal out LOW.

Assuming that the ACCEPT signal into Stage F remains LOW, data upstream of Stage F can continue to be shifted between stages and within stages on the respective clock phases until the next valid data block D3 reaches the primary storage elements of Stage E. As illustrated, this condition is reached during the ø1 phase of Cycle 4.

During the ø0 phase of Cycle 5, data D3 has been loaded into the primary storage element of Stage E. Since this data cannot be shifted further, the ACCEPT signal out of the primary storage elements of Stage E is set LOW. Upstream data can be shifted as normal.

Assume now, as in Cycle 5 of Fig. 2, that the device connected downstream of the pipeline is able to accept pipeline data. It signals this event by setting the ACCEPT signal into pipeline Stage F HIGH during the ø1 phase of Cycle 4. The primary storage elements of Stage F can now shift data to the right and they are also able to accept new data. Hence, the data D1 was shifted out during the ø1 phase of Cycle 5 so that the primary storage elements of Stage F no longer contain data that must be saved. During the ø1 phase of Cycle 5, the data D2 is, therefore, shifted within Stage F from the secondary storage elements to the primary storage elements. The secondary storage elements of Stage F are also able to accept new data and signal this by setting the ACCEPT signal into the primary storage elements of Stage E HIGH. During transfer of data within a stage, that is, from its secondary to its primary storage elements, both sets of storage elements will contain the same data, but the data in the secondary storage elements can be overwritten with no data loss since this data will also be held in the primary storage elements. The same holds true for data transfer from the primary storage elements of one stage into the secondary

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storage elements of a subsequent stage.

Assume now, that the ACCEPT signal into the primary storage elements of Stage F goes LOW during the ø1 phase in Cycle 5. This means that Stage F is not able to transfer the data D2 out of the pipeline. Stage F, consequently, sets the ACCEPT signal from its primary to its secondary storage elements LOW to prevent overwriting of the valid data D2. The data D2 stored in the secondary storage elements of Stage F, however, can be overwritten without loss, and the data D3, 10 is therefore, transferred into the secondary storage elements of Stage F during the ø0 phase of Cycle 6. Data D4 and D5 can be shifted downstream as normal. Once valid data D3 is stored in Stage F along with data D2, as long as the ACCEPT signal into the primary storage elements of Stage F is LOW, neither of the secondary storage elements can accept new data, and it signals this by setting the ACCEPT signal into Stage E LOW.

When the ACCEPT signal into the pipeline from the downstream device changes from LOW to HIGH or vice versa, this change does not have to propagate upstream within the pipeline further than to the immediately preceding storage elements (within the same stage or within the preceding pipeline stage). Rather, this change propagates upstream within the pipeline one storage element block per clock phase.

As this example illustrates, the concept of a "stage" in the pipeline structure illustrated in Fig. 3 is to some extent a matter of perception. Since data is transferred within a stage (from the secondary to the primary storage elements) as it is between stages (from the primary storage elements of the upstream stage into the secondary storage elements of the neighboring downstream stage), one could just as well consider a stage to consist of "primary" storage elements followed by "secondary storage elements" instead of

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as illustrated in Fig. 3. The concept of "primary" and "secondary" storage elements is, therefore, mostly a question of labeling. In Fig. 3, the "primary" storage elements can also be referred to as "output" storage elements, since they are the elements from which data is transferred out of a stage into a following stage or device, and the "secondary" storage elements could be "input" storage elements for the same stage.

In explaining the forementioned embodiments, as shown in Figs. 1-3, only the transfer of data under the control of the ACCEPT and VALID signals has been mentioned. It is to be further understood that each pipeline stage may also process the data it has received arbitrarily before passing it between its internal storage elements or before passing it to the following pipeline stage. Therefore, referring once again to Fig. 3, a pipeline stage can, therefore, be defined as the portion of the pipeline that contains input and output storage elements and that arbitrarily processes data stored in its storage elements.

Furthermore, the "device" downstream from the pipeline Stage F, need not be some other type of hardware structure, but rather it can be another section of the same or part of another pipeline. As illustrated below, a pipeline stage can set its ACCEPT signal LOW not only when all of the downstream storage elements are filled with valid data, but also when a stage requires more than one clock phase to finish processing its data. This also can occur when it creates valid data in one or both of its storage elements. In other words, it is not necessary for a stage simply to pass on the ACCEPT signal based on whether or not the immediately downstream storage elements contains valid data that cannot be passed on. Rather the ACCEPT signal itself may also be altered within the stage or, by circuitry external to the stage, in order to control the passage of data between adjacent storage

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elements. The VALID signal may also be processed in an analogous manner.

A great advantage of the two-wire interface (one wire for each of the VALID and ACCEPT signals) is its ability to control the pipeline without the control signals needing to propagate back up the pipeline all the way to its beginning stage. Referring once again to Fig. 1, Cycle 3, for example, although stage F "tells" stage E that is cannot accept data, and stage E tells stage D, and stage D tells stage C. Indeed, it there had been more stages containing valid data, then this signal would have propagated back even further along the pipeline. In the embodiment shown in Fig. 3, Cycle 3, the LOW ACCEPT signal is not propagated any further upstream than to Stage E and, then, only to its primary storage elements.

As described below, this embodiment is able to achieve this flexibility without adding significantly to the silicon area that is required to implement the design. Typically, each latch in the pipeline used for data storage requires only a single extra transistor (which lays out very efficiently in silicon). In addition, two extra latches and a small number of gates are preferably added to process the ACCEPT and VALID signals that are associated with the data latches in each half-stage.

Fig. 4 illustrates a hardware structure that implements a stage as shown in Fig. 3.

By way of example only, it is assumed that eight-bit data is to be transferred (with or without further manipulation in optional combinatorial logic circuits) in parallel through the pipeline. However, it will be appreciated that either more or less than eight-bit data can be used in practicing the invention. Furthermore, the two-wire interface in accordance with the embodiment is, however, suitable for use with any data bus width, and the data bus width may even

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change from one stage to the next if a particular application so requires. The interface in accordance with this embodiment can also be used to process analog signals.

As discussed previously, while other conventional timing arrangements may be used, the interface is preferably controlled by a two-phase, non-overlapping clock. In Figs. 4-9, these clock phase signals are referred to as PH0 and PH1. In Fig. 4, a line is shown for each clock phase signal.

Input data enters a pipeline stage over a multi-bit data bus IN_DATA and is transferred to a following pipeline stage or to subsequent receiving circuitry over an output data bus OUT_DATA. The input data is first loaded in a manner described below into a series of input latches (one of each input data signal) collectively referred to as LDIN, which constitute the secondary storage elements described above.

In the illustrated example of this embodiment, it is assumed that the Q outputs of all latches follow their D inputs, that is, they are "loaded", when the clock input is HIGH, i.e., at a logic "1" level. Additionally, the Q outputs hold their last values. In other words, the Q outputs are "latched" on the falling edge of their respective clock signals. Each latch has for its clock either one of two non-overlapping clock signals PH0 and PH1 (as shown in Fig. 5), or the logical AND combination of one of these clock signals PH0, PH1 and one logic signal. The invention works equally well, however, by providing latches that latch on the rising edges of the clock signals, or any other known latching arrangement, as long as conventional methods are applied to ensure proper timing of the latching operations.

The output data from the input data latch LDIN passes via an arbitrary and optional combinatorial logical circuit B1, which may be provided to convert output data from input latch LDIN into intermediate data, which is then later loaded in an output latch LDOUT, which comprises the primary storage

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elements described above. The output from the output data latch LDOUT may similarly pass through an arbitrary and optional combinatorial logic circuit B2 before being passed onward as OUT_DATA to the next device downstream. This may be another pipeline stage or any other device connected to the pipeline.

In the practice of the present invention, each stage of the pipeline also includes a validation input latch LVIN, a validation output latch LVOUT, an acceptance input latch LAIN, and an acceptance output latch LAOUT. Each of these four latches is, preferably, a simple, single-stage latch. The outputs from latches LVIN, LVOUT, LAIN and LAOUT are, respectively, QVIN, QVOUT, QAIN, QAOUT. The output signal QVIN from the validation input latch is connected either directly as an input to the validation output latch LVOUT, or via intermediate logic devices or circuits that may alter the signal.

Similarly, the output validation signal QVOUT of a given stage may be connected either directly to the input of the validation input latch QVIN of the following stage, or via intermediate devices or logic circuits, which may alter the validation signal. This output QVIN is also connected to a logic gate (to be described below), whose output is connected to the input of the acceptance input latch LAIN. The output QAOUT from the acceptance output latch LAOUT is connected to a similar logic gate (described below), optionally via another logic gate.

As shown in Fig. 4, the output validation signal QVOUT forms an OUT_VALID signal that can be received by subsequent stages as an IN_VALID signal, or simply to indicate valid data to subsequent circuitry connected to the pipeline. The readiness of the following circuit or stage to accept data is indicated to each stage as the signal OUT_ACCEPT, which is connected as the input to the acceptance output latch LAOUT,

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preferably via logic circuitry, which is described below. Similarly, the output QAOUT of the acceptance output latch LAOUT is connected as the input to the acceptance input latch LAIN, preferably via logic circuitry, which is described below.

In practicing the present invention, the out signals QVIN, QVOUT from the validation latches LVIN, LVOUT are combined with the acceptance signals QAOUT, OUT_ACCEPT, respectively, to form the inputs to the acceptance latches LAIN, LAOUT, respectively. In the embodiment illustrated in Fig. 4, these input signals are formed as the logical NAND combination of the respective validation signals QVIN, QVOUT, with the logical inverse of the representative acceptance output signals QAOUT, OUT_ACCEPT. Conventional logic gates, NAND1 and NAND2, perform the NAND operation, and the inverters INV1, INV2 form the logical inverses of the respective acceptance signals.

As is well known in the art of digital design, the output from a NAND gate is a logical "1" when any or all of its input signals are in the logical "0" state. The output from a NAND gate is, therefore, a logical "0" only when all of its inputs are in the logical "1" state. Also well known in the art, is that the output of a digital inverter such as INV1 is a logical "1" when its input signal is a "0" and is a "0" when its input signal is a "1"

The inputs to the NAND gate NAND1 are, therefore, QVIN and NOT (QAOUT), where "NOT" indicates binary inversion. Using known techniques, the input to the acceptance latch LAIN can be resolved as follows:

NAND(QVIN, NOT(QAOUT)) = NOT (QVIN) OR QAOUT

In other words, the combination of the inverter INV1 and the NAND gate NAND1 is a logical "1" either when the signal QVIN is a "0" or the signal QAOUT is a "1, or both. The gate NAND1 and the inverter INV1 can, therefore, be

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implemented by a single OR gate that has one of its inputs tied directly to the QAOUT output of the acceptance latch LAOUT and its other input tied to the inverse of the output signal QVIN of the validation input latch LVIN.

As is well known in the art of digital design, many latches suitable for use as the validation and acceptance latches may have two outputs, Q and NOT (Q), that is, Q and its logical inverse. If such latches are chosen, the one input to the OR gate can, therefore, be tied directly to the NOT (Q) output of the validation latch LVIN. The gate NAND1 and the inverter INV1 can be implemented using well known conventional techniques. Depending on the latch architecture used, however, it may be more efficient to use a latch without an inverting output, and to provide instead the gate NAND1 and the inverter INV1, both of which also can be implemented efficiently in a silicon device. Accordingly, any known arrangement may be used to generate the Q signal and/or its logical inverse.

The data and validation latches LDIN, LDOUT, LVIN and LVOUT, load their respective data inputs when both clock signals (PHO at the input side and PH1 at the output side) and the output from the acceptance latch of the same side are logical "1". Thus, the clock signal (PHO for the input latches LDIN and LVIN) and the output of the respective acceptance latch (in this case, LAIN) are used in a logical AND manner and data is loaded only when they are both logical "1".

In particular applications, such as CMOS implementations of the latches, the logical AND operation that controls the loading (via the illustrated CK or enabling "input") of the latches can be implemented easily in a conventional manner by connecting the respective enabling input signals (for example, PHO and QAIN for the latches LVIN and LDIN), to the gates of MOS transistors connected in series in the input

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lines of the latches. Consequently, is necessary to provide an actual logic AND gate, which might cause problems of timing due to propagation delay in high-speed applications. The AND gate shown in the Fig.s, therefore, only indicates the logical function to be performed in generating the enable signals of the various latches.

Thus, the data latch LDIN loads input data only when PHO and QAIN are both "1". It will latch this data when either of these two signals goes to a "0".

Although only one of the clock phase signals PHO and PH1, is used to clock the data and validation latches at the input (and output) side of the pipeline stage, the other clock phase signal is used, directly, to clock the acceptance latch at the same side. In other words, the acceptance latch on either side (input or output) of a pipeline stage is preferably clocked "out of phase" with the data and validation latches on the same side. For example, PH1 is used to clock the acceptance input latch, although PH0 is used in generating the clock signal CK for the data latch LDIN and the validation latch LVIN.

As an example of the operation of a pipeline augmented by the two-wire validation and acceptance circuitry assume that no valid data is initially presented at the input to the circuit, either from a preceding pipeline stage, or from a transmission device. In other words, assume that the validation input signal IN_VALID to the illustrated stage has not gone to a "1" since the system was most recently reset. Assume further that several clock cycles have taken place since the system was last reset and, accordingly, the circuitry has researched a steady-state condition. The validation input signal QVIN from the validation latch LVIN is, therefore, loaded as a "0" during the next positive period of the clock PH0. The input to the acceptance input latch LAIN (via the gate NAND1 or another equivalent gate),

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is, therefore, loaded as a "1" during the next positive period of the clock signal PH1. In other words, since the data in the data input latch LDIN is not valid, the stage signals that it is ready to accept input data (since it does not hold any data worth saving).

In this example, note that the signal IN_ACCEPT is used to enable the data and validation latches LDIN and LVIN. Since the signal IN_ACCEPT at this time is a "1", these latches effectively work as conventional transparent latches so that whatever data is on the IN_DATA bus simply is loaded into the data latch LDIN as soon as the clock signal PH0 goes to a "1". Of course, this invalid data will also be loaded into the next data latch LDOUT of the following pipeline stage as long as the output QAOUT from its acceptance latch is a "1".

Hence, as long as a data latch does not contain valid data, it accepts or "loads" any data presented to it during the next positive period of its respective clock signal. On the other hand, such invalid data is not loaded in any stage for which the acceptance signal from its corresponding acceptance latch is low (that is, a "0"). Furthermore, the output signal from a validation latch (which forms the validation input signal to the subsequent validation latch) remains a "0" as long as the corresponding IN_VALID (or QVIN) signal to the validation latch is low.

When the input data to a data latch is valid, the validation signal IN_VALID indicates this by rising to a "1". The output of the corresponding validation latch then rises to a "1" on the next rising edge of its respective clock phase signal. For example, the validation input signal QVIN of latch LVIN rises to a "1" when its corresponding IN_VALID signal goes high (that is, rises to a "1") on the next rising edge of the clock phase signal PH0.

Assume now, instead, that the data input latch LDIN contains valid data. If the data output latch LDOUT is ready

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to accept new data, its acceptance signal QAOUT will be a "1". In this case, during the next positive period of the clock signal PH1, the data latch LDOUT and validation latch LVOUT will be enabled, and the data latch LDOUT will load the data present at its input. This will occur before the next rising edge of the other clock signal PH0, since the clock signals are non-overlapping. At the next rising edge of PH0, the preceding data latch (LDIN) will, therefore, not latch in new input data from the preceding stage until the data output latch LDOUT has safely latched the data transferred from the latch LDIN.

Accordingly, the same sequence is followed by every adjacent pair of data latches (within a stage or between adjacent stages) that are able to accept data, since they will be operating based on alternate phases of the clock. Any data latch that is not ready to accept new data because it contains valid data that cannot yet be passed, will have an output acceptance signal (the QA output from its acceptance latch LA) that is LOW, and its data latch LDIN or LDOUT will not be loaded. Hence, as long as the acceptance signal (the output from the acceptance latch) of a given stage or side (input or output) of a stage is LOW, its corresponding data latch will not be loaded.

Fig. 4 also shows a reset feature included in a preferred embodiment. In the illustrated example, a reset signal NOTRESET0 is connected to an inverting reset input R (inversion is hereby indicated by a small circle, as is conventional) of the validation output latch LVOUT. As is well known, this means that the validation latch LVOUT will be forced to output a "0" whenever the reset signal NOTRESET0 becomes a "0". One advantage of resetting the latch when the reset signal goes low (becomes a "0") is that a break in transmission will reset the latches. They will then be in their "null" or reset state whenever a valid transmission

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begins and the reset signal goes HIGH. The rest signal NOTREST0, therefore, operates as a digital "ON/OFF" switch, such that it must be at a HIGH value in order to activate the pipeline.

Note that it is not necessary to reset all of the latches that hold valid data in the pipeline. As depicted in Fig. 4, the validation input latch LVIN is not directly reset by the reset signal NOTRESETO, but rather is reset indirectly. Assume that the reset signal NOTRESETO drops to a "0". The validation output signal QVOUT also drops to a "0", regardless of its previous state, whereupon the input to the acceptance output latch LAOUT (via the gate NAND1) goes HIGH. The acceptance output signal QAOUT also rises to a "I". This QAOUT value of "1" is then transferred as a "1" to the input of the acceptance input latch LAIN regardless of the state of the validation input signal QVIN. The acceptance input signal QAIN then rises to a "1" at the next rising edge of the clock signal PH1. Assuming that the validation signal IN_VALID has been correctly reset to a "0", then upon the subsequent rising edge of the clock signal PH0, the output from the validation latch LVIN will become a "0", as it would have done if it had been reset directly.

As this example illustrates, it is only necessary to reset the validation latch in only one side of each stage (including the final stage) in order to reset all validation latches. In fact, in many applications, it will not be necessary to reset every other validation latch: If the reset signal NOTRESET0 can be guaranteed to be low during more than one complete cycle of both phases PH0, PH1 of the clock, then the "automatic reset" (a backwards propagation of the rest signal) will occur for validation latches in preceding pipeline stages. Indeed, if the reset signal is held low for at least as many full cycles of both phases of the clock as there are pipeline stages, it will only be

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Register Name	Size/Dir	Reset State	Description
non_aligned_start_event	1 rw	0	When ignore_non_aligned is set to 1, start codes that are not byte aligned are ignored (treated as normal data) When ignore_non_aligned is set to 0, H.261 and MPEG start codes will be detected regardless of byte alignment and the non-aligned start event will be generated. If the mask register is set to 1 then the event will cause an interrupt and the start code detector will stop. See A.11.6. If the coding standard is configured as JPEG Ignore_non_aligned is ignored and the non-aligned start event will never be generated.
non_aligned_start_mask	1 rw	0	
Ignore_non_aligned	1 rw	0	
discard_extension_data	1 rw	0	When these registers are set to 1 extension or user data that cannot be decoded by the Spatial Decoder is discarded by the start code detector. See A.11.3.3.
discard_user_data	1 rw	0	
discard_all_data	1 rw	0	When set to 1 all data and Tokens are discarded by the start code detector. This continues until a **FLUSH** Token is supplied or the register is set to 0 directly. The **FLUSH** Token that resets this register is discarded and not output by the start code detector. See A.11.5.1 .
Insert_sequence_start	1 rw		See A.11.7

Table A.11.1 Start code detector Registers (Sheet 4 of 5)

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Register Name	Size/Dir.	Reset State	Description
start_code_search	3 rw	5	When this register is set to 0 the start code detector operates normally. When set to a higher value the start code detector discards data until the specified type of start code is detected. When the specified start code is detected the register is set to 0 and normal operation follows. See A.11.8 .
start_code_detector_coding_standard	2 rw	0	This register configures the coding standard used by the start code detector. The register can be loaded directly or by using a **CODING_STANDARD** Token. Whenever the start code detector generates a **CODING_STANDARD** Token (see A.11.7.4 on page 109) it carries its current coding standard configuration. This Token will then configure the coding standard used by all other parts of the decoder chip-set. See A.21.1 on page 180 and A.11.7.
picture_number	4 rw	0	Each time the start coded detector detects a picture start code in the data stream (or the H.261 or JPEG equivalent) a PICTURE_START Token is generated which carries the current value of picture_number. This register then increments.

Table A.11.1 Start code detector Registers (Sheet 5 of 5)

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Register Name	Size/Dir.	Reset State	Description
length_count	16 r0	0	This register contains the current value of the JPEG length count. This register is modified under the control of the coded data clock and should only be read via the MPI when the start code detector is stopped.

Table A.11.2 Start code detector test registers

A.11.3 Conversion of start codes to Tokens

In normal operation the function of the Start Code Detector is to identify start codes in the data stream and to then convert them to the appropriate start code Token. In the simplest case, data is supplied to the Start code Detector in a single long DATA Token. The output of the Start Code Detector is a number of shorter DATA Tokens interleaved with start code Tokens.

Alternatively, in accordance with the present invention, the input data to the Start Code Detector could be divided up into a number of shorter DATA Tokens. There is no restriction on how the coded data is divided into DATA Tokens other than that each DATA Token must contain 8 x n bits where n is an integer.

Other Tokens can be supplied directly to the input of the Start Code Detector. In this case, the Tokens are passed through the Start Code Detector with no processing

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to other stages of the Spatial Decoder. These Tokens can only be inserted just before the location of a start code in the coded data.

A.11.3.1 Start code formats

Three different start code formats are recognized by the Start Code Detector of the present invention. This is configured via the register, start_code_detector_coding_standard.

Coding Standard	Start Code Pattern (hex)	Size of start code value
MPEG	0x00 0x00 0x01 <value>	8 bit
JPEG	0xFF <value>	8 bit
H.261	0x00 0x01 <value>	4 bit

Table A.11.3 Start code formats

A.11.3.2 Start code Token equivalents

Having detected a start code, the Start Code Detector studies the value associated with the start code and generates an appropriate Token. In general, the Tokens are named after the relevant MPEG syntax. However, one of ordinary skill in the art will appreciate that the Tokens can follow additional naming formats. The coding standard currently selected configures the relationship between start code value and the Token generated. This relationship is shown in Table A.11.4.

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Start code Token generated	Start Code Value			
	MPEG (hex)	H.261 (hex)	JPEG (hex)	JPEG (name)
PICTURE_START	0x00	0x00	0xDA	SOS
SLICE_START[a]	0x01 to 0xAF	0x01 to 0x0C	0xDA to 0xD7	RST_0 to RST_7
SEQUENCE_START	0xB3		0xB8	SOI
SEQUENCE_END	0xB7		0xD9	EOI
GROUP_START	0xB8		0xC0	SOF_0[b]
USER_DATA	0XB2		0XE0 to 0xEF	APP_0 to APP_F
			0XFE	COM
EXTENSION_DATA	0xB5		0xC8	JPEG
			0xF0 to 0xFD	JPG_0 to JPG_0
			0x02 to 0xBF	RES
			0xC1 to 0xCB	SOF_1 to SOF_{11}
			0xCC	DAC
DHT_MARKER			0xC4	DHT
DNL_MARKER			0xDC	DNL
DQT_MARKER			0xDB	DQT
DRI_MARKER			0xDD	DRI

Table A.11.4 Tokens from start code values

a. This Token contains an 8 bit data field which is loaded with a value determined by the start code value.

b. Indicates start of baseline DCT encoded data.

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oriented) systems. Start codes in MPEG data should normally be byte aligned. However, the standard is designed to be allow bit serial searching for start codes (no MPEG bit pattern, with any bit alignment, will look like a start code, unless it is a start code). So, an MPEG decoder can be designed that will tolerate loss of byte alignment in serial data communications.

If a non-aligned start code is found, it will normally indicate that a communication error has previously occurred. If the error is a "bit-slip" in a bit-serial communications system, then data containing this error will have already been passed to the decoder. This error is likely to cause other errors within the decoder. However, new data arriving at the Start Code Detector can continue to be decoded after this loss of byte alignment.

By setting ignore_non_aligned = 0 and non_aligned_start_mask = 1, an interrupt can be generated if a non-aligned start code is detected. The response will depend upon the application. All subsequent start codes will be non-aligned (until byte alignment is restored). Accordingly, setting non_aligned_start_mask = 0 after byte alignment has been lost may be appropriate.

	MPEG	JPEG	H.251
ignore_non_aligned	0	1	0
non_aligned_start_mask	1	0	0

Table A.11.5 Configuring for byte alignment

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SECTION A.14 Video Demux

The Video Demux or Video parser as it is also called, completes the task of converting coded data into Tokens started by the Start Code Detector. There are four main processing blocks in the Video Demux: Parser State Machine, Huffman decoder (including an ITOD), Macroblock counter and ALU.

The Parser or state machine follows the syntax of the coded video data and instructs the other units. The Huffman decoder converts variable length coded (VLC) data into integers. The Macroblock counter keeps track of which section of a picture is being decoded. The ALU performs the necessary arithmetic calculations.

A.14.1 Video Demux registers

Register name	Size/Dir.	Reset State	Description
demux_access *CED_H_CTRL[7]*	1 rw	0	This access bit stops the operation of the Video Demux so that it's various registers can be accessed reliably. See A.6 4.1.
huffman_error_code *CED_H_CTRL[6:4]*	3 ro		When the Video Demux stops following the generation of a huffman_event interrupt request this 3 bit register holds a value indicating why the interrupt was generated. See A.14.5.1.
parser_error_code *CED_H_DMUX_ERR*	8 ro		When the Video Demux stops following the generation of a parser_event interrupt request this 8 bit register holds a value indicating why the interrupt was generated. See A.14.5.2 .
demux_keyhole_address *CED_H_KEYHOLE_ADDR*	12 rw	x	Keyhole access to the Video Demux's extended address space. See A 6.4.3 for more information about accessing registers through a keyhole.
demux_keyhole_data *CED_H_KEYHOLE*	8 rw	x	Tables A.14 2, A.14.3 and A.14.4 describe the registers that can be accessed via the keyhole.

Table A.14.1 Top level Video Demux registers

COPY

Register name	Size/Dir.	Reset State	Description
dummy_last_picture *CED_H_ALU_REG0* *r_rom_control* *r_dummy_last_frame_bit*	1 rw	0	When this register is set to 1 the Video Demux will generate information for a "dummy" intra picture as the last picture of an MPEG sequence. This function is useful when the Temporal Decoder is configured for automatic picture re-ordering (see A.18.3.5, "Picture sequence re-ordering") to flush the last P or I picture out of the Temporal Decoder. No "dummy" picture is required if: • the Temporal Decoder is not configured for re-ordering • another MPEG sequence will be decoded immediately (as this will also flush out the last picture) • the coding standard is not MPEG
field_info *CED_H_ALU_REG0* *r_rom_control* *r_field_info_bit*	1 rw	0	When this register is set to 1 the first byte of any MPEG extra_information_picture is placed in the FIELD_INFO Token. See A.14.7.1.
continue *CED_H_ALU_REG0* *r_rom_control* *r_field_continue_bit*	1 rw	0	This register allows user software to control how much extra, user or extension data it wants to receive when it is detected by the decoder. See A.14.6 and A.14.7 .
rom_revision *CED_H_ALU_REG1* *r_rom_revision*	8 ro		Immediately following reset this holds a copy of the microcode ROM revision number. This register is also used to present to control software data values read from the coded data. See A.14.6, "Receiving User and Extension data", on page 148 and A.14.7, "Receiving Extra Information".

Table A.14.1 Top level Video Demux registers (contd)

COPY

Register name	Size/Dir.	Reset State	Description
huffman_event	1 rw	0	A Huffman event is generated if an error is found in the coded data See A.14.5.1 for a description of these events. If the mask register is set to 1 then an interrupt can be generated and the Video Demux will stop. If the mask register is set to 0 then no interrupt is generated and the Video Demux will attempt to recover from the error.
huffman_mask	1 rw	0	
parser_event	1 rw	0	A Parser event can be in response to errors in the coded data or to the arrival of information at the Video Demux that requires software intervention. See A.14 5.2 for a description of these events. If the mask register is set to 1 then an interrupt can be generated and the Video Demux will stop. If the mask register is set to 0 then no interrupt is generated and the Video Demux will attempt to continue.
parser_mask	12 rw	x	

Table A.14.1 Top level Video Demux registers (contd)

Register name	size/dir.	Reset State	Description
component_name_0 component_name_1 component_name_2 component_name_3	8 rw	x	During JPEG operation the register component_name_*n* holds an 8 bit value indicating (to an application) which colour component has the component ID *n*.
horiz_pels	16 rw	x	These registers hold the horizontal and vertical dimensions of the video being decoded in pixels. See section A.14.2 .
vert_pels	16 rw	x	
horiz_macroblocks	16 rw	x	These registers hold the horizontal and vertical dimensions of the video being decoded in macroblocks. See section A.14.2 .
vert_macroblocks	16 rw	x	

Table A.14.2 video demux picture construction registers

COPY

Register name	Size/Dir.	Reset State	Description
max_h	2 rw	x	These registers hold the macroblock width and height in blocks (8 x 8 pixels). The values 0 to 3 indicate a width/height of 1 to 4 blocks See section A.14.2 .
max_v	2 rw	x	
max_component_id	2 rw	x	The values 0 to 3 indicate that 1 to 4 different video components are currently being decoded. See section A.14.2 .
Nf	8 rw	x	During JPEG operation this register holds the parameter Nf (number of image components in frame).
blocks_h_0 blocks_h_1 blocks_h_2 blocks_h_3	2 rw	x	For each of the 4 colour components the registers blocks_h_*n* and blocks_v_*n* hold the number of blocks horizontally and vertically in a macroblock for the colour component with component ID *n*. See section A.14.2 .
blocks_v_0 blocks_v_1 blocks_v_2 blocks_v_3	2 rw	x	
tq_0 tq_1 tq_2 tq_3	2 rw	x	The two bit value held by the register tq_*n* describes which inverse Quantisation table is to be used when decoding data with component ID *n*.

Table A.14.2 video demux picture construction registers (contd)

COPY

Register Name	Size/Dir.	Reset State	Description
dc_huff_0 dc_huff_1 dc_huff_2 dc_huff_3	2 rw		The two bit value held by the register dc_huff_*n* describes which Huffman decoding table is to be used when decoding the DC coefficients of data with component ID *n*. Similarly ac_huff_*n* describes the table to be used when decoding AC coefficients. Baseline JPEG requires up to two Huffman tables per scan. The only tables implemented are 0 and 1.
ac_huff_0 ac_huff_1 ac_huff_2 ac_huff_3	2 rw		
dc_bits_0[15:0] dc_bits_1[15:0]	8 rw		Each of these is a table of 16, eight bit values. They provide the BITS information (see JPEG Huffman table specification) which form part of the description of two DC and two AC Huffman tables. See section A.14.3.1 .
ac_bits_0[15:0] ac_bits_1[15:0]	8 rw		
dc_huffval_0[11:0] dc_huffval_1[1:0]	8 rw		Each of these is a table of 12, eight bit values. They provide the HUFFVAL information (see JPEG Huffman table specification) which form part of the description of two AC Huffman tables. See section A.14.3.1 .
ac_huffval_0(161:0) ac_huffval_1(161:0)	8 rw		Each of these is a table of 162, eight bit values. They provide the HUFFVAL information (see JPEG Huffman table specification) which form part of the description of two DC Huffman tables. See section A.14.3.1 .
dc_zssss_0 dc_zssss_1	8 rw		These 8 bit registers hold values that are "special cased" to accelerate the decoding of certain frequency used JPEG VLCs. dc_ssss - magnitude of DC coefficient is 0. ac_eob - end of block ac_zrl - run of 16 zeros
ac_eob_0 ac_eob_1	8 rw		
ac_zrl_0 ac_zrl_1	8 rw		

Table A.14.3 Video demux Huffman table registers

COPY

Register Name	Size/Dir.	Reset State	Description
buffer_size	10 rw		This register is loaded when decoding MPEG data with a value indicating the size of VBV buffer required in an *ideal* decoder. This value is not used by the decoder chips. However, the value it holds may be useful to user software when configuring the coded data buffer size and to determine whether the decoder is capable of decoding a particular MPEG data file.
pel_aspect	4 rw		This register is loaded when decoding MPEG data with a value indicating the pel aspect ratio. The value is a 4 bit integer that is used as an index into a table defined by MPEG. See the MPEG standard for a definition of this table. This value is not used by the decoder chips. However, the value it holds may be useful to user software when configuring a display or output device.
bit_rate	4 rw		This register is loaded when decoding MPEG data with a value indicating the coded data rate. See the MPEG standard for a definition of this value. This value is not used by the decoder chips. However, the value it holds may be useful to user software when configuring the decoder start-up registers.
pic_rate	4 rw		This register is loaded when decoding MPEG data with a value indicating the picture rate. See the MPEG standard for a definition of this value. This value is not used by the decoder chips. However, the value it holds may be useful to user software when configuring a display or output device.
Constrained	1 rw		This register is loaded when decoding MPEG data to indicate if the coded data meets MPEG's constrained parameters. See the MPEG standard for a definition of this flag. This value is not used by the decoder chips. However, the value it holds may be useful to user software to determine whether the decoder is capable of decoding a particular MPEG data file.

COPY

Register Name	Size/Dir.	Resel State	Description
picture_type	2 rw		During MPEG operation this register holds the picture type of the picture being decoded.
h_261_pic_type	8 rw		This register is loaded when decoding H.261 data. It holds information about the picture format. 7 6 5 4 3 2 1 0 f f s d f d f f Flags: s - Split Screen Indicator d - Document Camera r - Freeze Picture Release This value is not used by the decoder chips. However, the information should be used when configuring horiz_pels, vert_pels and the display or output device.
broken_closed	2 rw		During MPEG operation this register holds the broken_link and closed_gap information for the group of pictures being decoded. 7 6 5 4 3 2 1 0 r r r r r r c b Flags: C – closed_gap

Table A.14.4 Other Video Demux registers (contd)

COPY

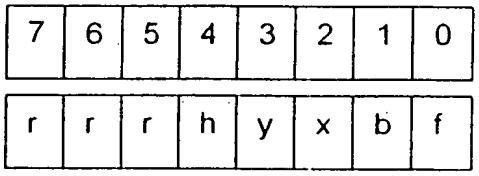
Register Name	Size/Dir.	Reset State	Description
Prediction_mode	5 rw		During MPEG and H.261 operation this register holds the current value of prediction mode.  Flags: h - enable H.261 loop filter y - reset backward vector prediction.
vbv_delay	16 rw		This register is loaded when decoding MPEF data with a value indicating the minimum start-up delay before decoding should start See the MPEG standard for a definition of this value. This value is not used by the decoder chips. However, the value it holds may be useful to user software when configuring the decoder start-up registers.
pic_number	8 rw		This register holds the picture number for the pictures that is currently being decoded by the Video Demux. This number was generated by the start code detector when this picture arrived there. See Table A.11.2 for a description of the picture number.
dummy_last_picture	1 rw	0	These registers are also visible at the top level. See Table A.14.1
field_info	1 rw	0	
continue	1 rw	0	
rom_revision	8 rw		
coding_standard	2 ro		This register is loaded by the CODING_STANDARD Token to configure the Video Demux's mode of operation See section A.21.1 .

Table A.14.4 Other Video Demux registers (contd)

COPY

Register name	Size/Dir.	Reset State	Description
restart_interval	8 rw		This register is loaded when decoding JPEG data with a value indicating the minimum start-up delay before decoding should start. See the MPEG standard for a definition of this value.

Table A.14.4 Other Video Demux registers (contd)

Register	Token	standard	comment
component_name_*n*	COMPONENT_NAME	JPEG	in coded data.
		MPEG	not used in standard
		H.261	
horiz_pels vert_pels	HORIZONAL_SIZE VERTICAL_SIZE	MPEG	in coded data.
		JPEG	
		H.261	automatically derived from picture type.
horiz_macroblocks vert_macroblocks	HORIZONTAL_MBS VERTICAL_MBS	MPEG	control software must derive from horizontal and vertical picture size.
		JPEG	
		H.261	automatically derived from picture type.
max_h max_v	DEFINE_MAX_SAMPLING	MPEG	control software must configure. Sampling structure is fixed by standard.
		JPEG	in coded data.
		H.261	automatically configured for 4:2:0 video.

5 **Table A.14.5 register to Token cross reference**

COPY

max_component_id	MAX_COMP_ID	MPEG	control software must configure. Sampling structure is fixed by standard.
		JPEG	in coded data.
		H.261	automatically configured for 4:2:0 video.
tq_0 tq_1 tq_2 tq_3	JPEG_TABLE_SELECT	JPEG	in coded data.
		MPEG	not used in standard.
		H.261	
blocks_h_0 blocks_h_1 blocks_h_2 blocks_h_3 blocks_v_0 blocks_v_1 blocks_v_2 blocks_v_3	DEFINE_SAMPLING	MPEG	control software must configure. sampling structure is fixed by standard.
		JPEG	in coded data.
		H.261	automatically configured for 4:2:0 video.
dc_huff_0 dc_huff_1 dc_huff_2 dc_huff_3	in scan header data	JPEG	in coded data.
	MPEG_DCH_TABLE	MPEG	control software must configure
		H.261	not used in standard.
ac_huff_0 ac_huff_1 ac_huff_2 ac_huff_3	in scan header data	JPEG	in coded data.
		MPEG	not used in standard.
		H.261	

Table a. 14.5 Register to Token cross reference (contd)

COPY

Register	Token	standard	comment
dc_bits_0[15:0] dc_bits_1[15:0]	in DATA Token following DHT_MARKER Token	JPEG	in coded data.
dc_huffval_0[11:0] dc_huffval_1[11:0] dc_zssss_0 dc_zssss_1		MPEG	control software must configure.
		H.261	not used in standard
ac_bits_0[15:0] ac_bits-1[15:0]	in DATA Token following DHT_MARKER Token	JPEG	in coded data.
ac_huffval_0[161:0] ac_huffval_1[161:0] ac_eob_0 ac_eob_1 ac_zrl_0 ac_zrl_1		MPEG	not used in standard.
		H.261	
buffer_size	VBV_BUFFER_SIZE	MPEG	in coded data.
		JPEG	not used in standard.
		H.261	
pel_aspect	PEL_ASPECT	MPEG	in coded data.
		JPEG	not used in standard.
		H.261	
bit _rate	BIT_RATE	MPEG	in coded data.
		JPEG	not used in standard.
		H.261	
pic_rate	PICTURE_RATE	MPEG	in coded data.
		JPEG	not used in standard.
		H.261	
constrained	CONSTRAINED	MPEG	in coded data.
		JPEG	not used in standard.
		H.261	
picture_type	PICTURE_TYPE	MPEG	in coded data.
		JPEG	not used in standard
		H.261	

Table A 14.5 Register to Token cross reference

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broken_closed	BROKEN_CLOSED	MPEG	in coded data.
		JPEG	not used in standard.
		H.261	
prediction_mode	PREDICTION_MODE	MPEG	in coded data.
		JPEG	not used in standard.
		H.261	
h_261_pic_type	PICTURE_TYPE (when standard is H.261)	MPEG	not relevant
		JPEG	
		H.261	in coded data.
vbv_delay	VBV_DELAY	MPEG	in coded data.
		JPEG	not used in standard.
		H.261	
pic_number	Carried by: PICTURE_START	MPEG	Generated by start code detector.
		JPEG	
		H.261	
coding_standard	CODING_STANDARD	MPEG	configured in start code by control software detector.
		JPEG	
		H.261	

Table A.14.5 Register to Token cross reference (contd)

A.14.2 Picture structure

In the present invention, picture dimensions are described to the Spatial Decoder in 2 different units: pixels and macroblocks. JPEG and MPEG both communicate picture dimensions in pixels. Communicating the dimensions in pixels determine the area of the buffer that contains the valid data; this may be smaller than the total buffer size. Communicating dimensions in macroblocks determines the size of buffer required by the decoder. The macroblock dimensions must be derived by the user from the pixel

COPY

dimensions. The Spatial Decoder registers associated with this information are: horiz_pels, vert_pels, horiz_macroblocks and vert_macroblocks.

The Spatial Decoder registers, blocks_h_*n*, blocks_v_*n*, max_h, max_v and max_component_id specify the composition of the macroblocks (minimum coding units in JPEG). Each is a 2 bit register than can hold values in the range 0 to 3. All except max_component_id specify a block count of 1 to 4. For example, if register max_h holds 1, then a macroblock is two blocks wide. Similarly, max_component_id specifies the number of different color components involved.

	2:1:1	4:2:2	4:2:0	1:1:1
max_h	1	1	1	0
max_v	0	1	1	0
max_component_id	2	2	2	2
blocks_h_0	1	1	1	0
blocks_h_1	0	0	0	0
blocks_h_2	0	0	0	0
blocks_h_3	x	x	x	x
blocks_v_0	0	1	1	0
blocks_v_1	0	1	0	0
blocks_v_2	0	1	0	0
blocks_v_3	x	x	x	x

Table A.14.6 Configuration for various macroblock formats

COPY

DATA and DHT_MARKER Tokens to the input of the Spatial Decoder while the Spatial Decoder is configured for JPEG operation. This mechanism can be used for configuring the DC coefficient Huffman tables required for MPEG operation, however, the coding standard of the Spatial Decoder must be set to JPEG while the tables are down loaded.

E	7	6	5	4	3	2	1	0	Token Name	
1	0	0	0	1	0	1	0	1	CODING_STANDARD	
0	0	0	0	0	0	0	0	1	1 = JPEG	
0	0	0	0	1	1	1	0	0	DHT_MARKER	
1	0	0	0	0	0	1	x	x	DATA	
1	t	t	t	t	t	t	t	t	T_n Value indicating which Huffman table is to be loaded. JPEG allows 4 tables to be downloaded. Values 0x00 and 0x01 specify DC coefficient coding tables 0 and 1. Values 0x10 and 0x11 specifies AC coefficient coding tables 0 and 1.	This sequence can be repeated to allow several tables to be described in a single Token.
1	n	n	n	n	n	n	n	n	L_i- 16 words carrying BITS information	
1	n	n	n	n	n	n	n	n		
1	n	n	n	n	n	n	n	n	V_{ij}- Words carrying HUFFVAL information (the number of words depends on the number of different symbols). e - the extension bit will be 0 if this is the end of the DATA Token or 1 if another table description is contained in the same DATA Token.	
				:						
e	n	n	n	n	n	n	n	n		

Table A.14.7 Huffman table configuration via Tokens

COPY

Addr. (hex)	Bit num.	Register Name	Page references
0x20	7:5	not used	
	4:0	page_start_length(4:0)	
0x21	7:4	not used	
	3:0	read_cycle_length(3:0)	
0x22	7:4	not used	
	3:0	write_cycle_length(3:0)	
0x23	7:4	not used	
	3:0	refresh_cycle_length(3:0)	
0x24	7:4	not used	
	3:0	CAS_falling(3:0)	
0x25	7:4	not used	
	3:0	RAS_falling(3:0)	
0x26	7:1	not used	
	0	interface_timing_access	
0x27	7:0	not used	
0x28	7:6	RAS_strength(2:0)	
	5:3	OEWE_strength(3:0)	
	2:0	DRAM_data_strength(3:0)	
0x29	7	not used	
	6:4	DRAM_addr_strength(3:0)	
	3:1	CAS_strength(3:0)	
	0	RAS_strength(3)	

Table A.17.9 DRAM interface configuration registers

COPY

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
DRAM_addr[4]	195	data[2]	143	vdd	91	DRAM_data[19]	39
vdd	194	nc	142	out_data[6]	90	DRAM_data[20]	38
DRAM_addr[5]	193	data[1]	141	out_data[7]	89	nc	37
DRAM_addr[6]	192	data[0]	140	nc	88	GND	36
nc	191	nc	139	out_extn	87	DRAM_data[21]	35
GND	190	vdd	138	GND	86	nc	34
DRAM_addr[7]	189	addr[7]	137	DRAM_data[0]	85	DRAM_data[22]	33
DRAM_addr[8]	188	addr[6]	136	DRAM_data[1]	84	vdd	32
vdd	187	addr[5]	135	DRAM_data[2]	83	DRAM_data[23]	31
DRAM_addr[9]	186	GND	134	vdd	82	DRAM_data[24]	30
nc	185	addr[4]	133	DRAM_data[3]	81	nc	29
DRAM_addr[10]	184	addr[3]	132	nc	80	GND	28
GND	183	addr[2]	131	DRAM_data[4]	79	DRAM_data[25]	27
nc	182	addr[1]	130	GND	78	nc	26
vdd	181	vdd	129	nc	77	DRAM_data[26]	25
test pin	180	addr[0]	128	DRAM_data[5]	76	nc	24
test pin	179	$\overline{\text{enable}}$[0]	127	nc	75	Vdd	23
test pin	178	$\overline{\text{enable}}$[1]	126	DRAM_data[6]	74	DRAM_data[27]	22
decoder_clock	177	$\overline{\text{rw}}$	125	vdd	73	nc	21
nc	176	GND	124	DRAM_data[7]	72	DRAM_data[28]	20
GND	175	test pin	123	nc	71	DRAM_data[29]	19
in_extn	174	test pin	122	DRAM_data[8]	70	GND	18
in_data[8]	173	trst	121	GND	69	DRAM_data[30	17
in_data[7]	172	tdo	120	DRAM_data[9]	68	nc	16
in_data[6]	171	nc	119	nc	67	DRAM_data[31]	15
vdd	170	vdd	118	DRAM_data[10]	66	vdd	14
in_data[5]	169	tms	117	vdd	65	nc	13
in_data[4]	168	tdi	116	nc	64	$\overline{\text{WE}}$	12
in_data[3]	167	tck	115	DRAM_data[11]	63	$\overline{\text{RAS}}$	11
in_data[2]	166	test pin	114	nc	62	nc	10
GND	165	GND	113	DRAM_data[12]	61	GND	9
in_data[1]	164	DRAM_enable	112	GND	60	$\overline{\text{CAS}}$[0]	8
in_data[0]	163	test pin	111	DRAM_data[13]	59	nc	7
in_valid	162	test pin	110	nc	58	$\overline{\text{CAS}}$[1]	6
in_accept	161	test pin	109	DRAM_data[14]	57	vdd	5

Table A.17.3 Temporal Decoder Pin Assignments (contd)

COPY

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
reset	160	nc	108	vDD	56	$\overline{CAS}$[2]	4
vDD	159	nc	107	nc	55	nc	3
nc	158	nc	106	nc	54	$\overline{CAS}$[3]	2
nc	157	nc	105	nc	53	nc	1

Table A.17.3 Temporal Decoder Pin Assignments (contd)

A.17.1.1 "nc" no connect pins

The pins labelled nc in Table A.17.3 are not currently used in the present invention and are reserved for future products. These pins should be left unconnected. They should not be connected to V_{DD}, GND, each other or any other signal.

A.17.1.2 V_{DD} and GND pins

As will be appreciated all the V_{DD} and GND pins provided must be connected to the appropriate power supply. The device will not operate correctly unless all the V_{DD} and GND pins are correctly used.

A.17.1.3 Test pin connections for normal operation

Nine pins on the Temporal Decoder are reserved for internal test use.

Pin number	Connection
	Connect to GND for normal operation
	Connect to V_{DD} for normal operation
	Leave Open Circuit for normal operation

Table A.17.4 Default test pin connections

COPY

and this ensures that other decoder chips (such as the Temporal Decoder) are correctly configured.

A.14.4.3 MPEG Huffman tables

The majority of the Huffman coding tables required to decode MPEG are held in ROMs within the Spatial Decoder (again, in the parser state machine) and, thus, require no user intervention. The exceptions are the tables required for decoding the DC coefficients of Intral macroblocks. Two tables are required, one for chroma the other for luma. These must be configured by user software before decoding begins.

Macroblock construction	CIF / QCIF	picture construction	CIF	QCIF
max_h	1	horiz_pels	352	176
max_v	1	vert_pels	288	144
max_component_id	2	horiz_macroblocks	22	11
blocks_h_0	1	vert_macroblocks	18	9
blocks_h_1	0			
blocks_h_2	0			
blocks_v_0	1			
blocks_v_1	0			
blocks_v_2	0			

Table A.14.8 Automatic settings for H.261

Table A.14.10 shows the sequence of Tokens required to configure the DC coefficient Huffman tables within the Spatial Decoder. Alternatively, the same results can be obtained by writing this information to registers via the MPI.

The registers dc_huff_*n* control which DC coefficient Huffman tables are used with each color component. Table

COPY

A.14.9 shows how they should be configured for MPEG operation. This can be done directly via the MPI or by using the MPEG_DCH_TABLE Token.

dc_huff_0	0
dc_huff_1	1
dc_huff_2	1
dc_huff_3	x

Table A.14.9 MPEG DC Huffman table selection via MPI

E	(7:0)	Token Name
1	0x15	CODING_STANDARD
0	0x01	1 = JPEG
0	0x1C	DHT_MARKER
1	0X04	DATA (could be any colour component. 0 is used in the example)
1	0X00	0 indicates that this Huffman table is DC coefficient coding table 0

Table A.14.10 MPEG DC Huffman table configuration

COPY

E	(7:0)	Token Name
1	0x00	16 words carrying BITS information a total of 9
1	0x02	
1	0x03	different VLCs:
1	0x01	2,2 bit codes
1	0x01	
1	0x01	3,3 bit codes
1	0x01	1,4 bit codes
1	0x00	
1	0x00	1,5 bit codes
1	0x00	1,6 bit codes
1	0x00	
1	0x00	1,7 bit codes
1	0x00	
1	0x00	If configuring via the MPI rather than with Tokens these values would be written into the dc_bits_0[15:0] registers.
1	0x00	
1	0x00	
1	0x01	9 words carrying HUFFVAL information
1	0x02	
1	0x00	If configuring via the MPI rather than with tokens these values would be written into the dc_huffval_0[11:0] registers.
1	0x03	
1	0x04	
1	0x05	
1	0x06	
1	0x07	
0	0x08	

Table A.14.10 MPEG DC Huffman table configuration (contd)

COPY

E	(7.0)	Token Name
0	0x1C	DHT_MARKER
1	0x04	DATA (could be any colour component, 0 is used in this example)
1	0x01	1 indicates that this Huffman table is DC coefficient coding table 1
1	0x00	16 words carrying BITS information describing a total of 9
1	0x03	
1	0x01	different VLCs:
1	0x01	3, 2 bit codes
1	0x01	
1	0x01	1, 3 bit codes
1	0x01	1, 4 bit codes
1	0x01	
1	0x00	1, 5 bit codes
1	0x00	
1	0x00	1, 6 bit codes
1	0x00	1, 7 bit codes
1	0x00	
1	0x00	1, 8 bit codes
1	0x00	
1	0x00	If configuring via the MPI rather than with Tokens these values would be written into the dc_bits_1[15:0] registers.
1	0x00	9 words carrying HUFFVAL information
1	0x01	
1	0x02	If configuring via the MPI rather than with Tokens these values would be
1	0x03	
1	0x04	written into the dc_huffval_1[11:0] registers.
1	0x05	
1	0x06	
1	0x07	
1	0x08	
1	0x04	MPEG_DCH_TABLE
0	0x00	Configure so table 0 is used for component 0
1	0x05	MPEG_DCH_TABLE
0	0x01	Configure so table 1 is used for component 1
1	0x06	MPEG_DCH_TABLE
0	0x01	Configure so table 1 is used for component 2

Table A.14.10 MPEG DC Huffman table configuration (contd)

COPY

E	(7:0)	Token Name
1	0x15	CODING_STANDARD
0	0x02	2 = JPEG

Table A.14.10 MPEG DC Huffman table configuration (contd)

A.14.4.4 MPEG Picture structure

The macroblock construction *defined* for MPEG is the same as that used by H.261. The picture dimensions are encoded in the coded data.

For standard 4:2:0 operation, the macroblock characteristics should be configured as indicated in Table A.14.8. This can be done either by writing to the registers as indicated or by applying the equivalent Tokens (see Table A.14.5) to the input of the Spatial Decoder.

The approach taken to configure picture dimensions will depend upon the application. If the picture format is known before decoding starts, then the picture construction registers listed in Table A.14.8 can be initialized with appropriate values. Alternatively, the picture dimensions can be decoded from the coded data and used to configure the Spatial Decoder. In this case the user must service the parser error ERR_MPEG_SEQUENCE, see A.14.8, "Changes at the MPEG sequence layer".

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huffman_error			Description
[2]	[1]	[0]	
0	0	0	No error. This error should not occur during normal operation
x	0	1	Failed to find terminal code in VLC within 16
x	1	0	Found serial data when Token expected.
x	1	1	Found Token when serial data expected.
1	x	x	Information describing more than 64 coefficients for a single block was decoded indicating a bitstream error. The block output by the Video Demux will contain only 64

Table A.14.11 Huffman error codes

parser_error_code(7:0)	Description
0x00	ERR_NO_ERROR No Parser error has occured, this event should not occur during
0x10	ERR_EXTENSION_TOKEN An EXTENSION_DATA Token has been detected by the Parser. The detection of this Token should precede a DATA Token that contains the extension data. See A.14.6 on page 148
0x11	ERR_EXTENSION_DATA Following the detection of an EXTENSION_DATA Token, a DATA Token containing the extension data has been detected. See A.14.6 on page 148
0x12	ERR_USER_TOKEN A USER_DATA Token has been detected by the Parser. The detection of this Token should preceed a DATA Token that contains the user data. See A.14.6 on page 148
0x13	ERR_USER_DATA Following the detection of a USER_DATA Token, a DATA Token containing the user data has been detected. See A.14.6 on page 148
0x20	ERR_PSPARE H.261 PSARE information has been detected see A.14.7 on page 149.

Table A.14.12 Parser error codes (Sheet 1 of 5)

COPY

0x21	ERR_GSPARE H.261 GSARE information has been detected see A.14.7 on page 149.
0x22	ERR_PTYPE The value of the H.261 picture type has changed. The register h_261_pic_type can be inspected to see what the new value is.
0x30	ERR_JPEG_FRAME
0x31	ERR_JPEG_FRAME_LAST
0x32	ERR_JPEG_SCAN Picture size or Ns changed
0x33	ERR_JPEG_SCAN_COMP Component Change!
0x34	ERR_DNL_MARKER
0x40	ERR_MPEG_SEQUENCE One of the parameters communicated in the MPEG sequence layer has changed. See A.14.8 on page 150.
0x41	ERR_EXTRA_PICTURE MPEG extra_information_picture has been detected see A.14.7 on page 149.
0x42	ERR_EXTRA_SLICE MPEG extra_information_slice has been detected see A.14.7 on page 149.
0x43	ERR_VBV_DELAY The VBV_DELAY parameter for the first picture in a *new* MPEG video sequence has been detected by the Video Demux. The new value of delay is available in the register vbv_delay. The first picture of a new sequence is defined as the first picture after a sequence end.FLUSH or reset.
0x80	ERR_SHORT_TOKEN An incorrectly formed Token has been detected. This error should not occur during normal operation.

Table A.14.12 Parser error codes (Sheet 2 of 5)

COPY

Parser_error_code (7:0)	Description
0x90	ERR_H261_PIC_END_UNEXPECTED During H.261 operation the end of a picture has been encountered at an unexpected position. This is likely to indicate an error in the coded data.
0x91	ERR_GN_BACKUP During H.261 operation a group of blocks has been encountered with a group number less than that expected. This is likely to indicate an error in the coded
0x92	ERR_GN_SKIP_GOB During H.261 operation a group of blocks has been encountered with a group number
0xA0	ERR_NBASE_TAB During JPEG operation there has been an attempt to down load a Huffman table that is not supported by baseline JPEG (baseline JPEG only supports tables 0 and 1 for entropy coding).
0xA1	ERR_QUANT_PRECISION During JPEG operation there has been an atternpt to down load a quantisation table that is not supported by baseline JPEG (baseline JPEG only supports 8 bit precision in
0xA2	ERR_SAMPLE_PRECISION During JPEG operation there has been an attempt to specify a sample precision greater than that supported by baseline JPEG (baseline JPEG only supports 8
0xA3	ERR_NBASE_SCAN One or more of the JPEG scan header parameters Ss, Se, Ah and Al is set to a value not supported by baseline JPEG (indicating spectral selection and/or successive
0xA4	ERR_UNEXPECTED_DNL During JPEG operation a DNL marker has been encountered in a scan that is not the first scan in a frame.
0xA5	ERR_EOS_UNEXPECTED During JPEG operation an EOS marker has been encountered in an unexpected place.

Table A.14.12 Parser error codes (Sheet 3 of 5)

COPY

Parser_code_error (7:0)	Description
0xA6	ERR_RESTART_SKIP During JPEG operation a restart marker has been encountered either in an unexpected place or the value of the restart marker is unexpected. If a restart marker is not found when one is expected the Huffman event "Found serial data when
0xB0	ERR_SKIP_INTRA During MPEG operation, a macro block with a macro block address increment greater than 1 has been found within an intra(1) picture. This is illegal and probably indicates a bitstream error.
0xB1	ERR_SKIP_DINTRA During MPEG operation, a macro block with a macro block address increment greater than 1 has been found within an DC only (D) picture. This is illegal and probably indicates a bitstream error.
0xB2	ERR_BAD_MARKER During MPEG operation, a marker bit did not have the expected value. This probably indicates a bitstream error.
0xB3	ERR_D_MBTYPE During MPEG operation, within a DC only (D) picture, a macroblock was found with a macroblock type other than 1. This is illegal and probably indicates a
0xB4	ERR_D_MBEND During MPEG operation, within a DC only (D) picture, a macroblock was found with 0 in it's end of macroblock bit. This is illegal and probably indicates a
0xB5	ERR_SVP_BACKUP During MPEG operation, a slice has been encountered with a slice vertical position less
0xB6	ERR_SVP_SKIP_ROWS During MPEG operation, a slice has been encountered with a slice vertical position greater than that expected. This is likely to indicate an error in the
0xB7	ERR_FST_MBA_BACKUP During MPEG operation, a macroblock has been encountered with a macro block address less than that expected. This is likely to indicate an error in the

Table A.14.12 Parser error codes (Sheet 4 of 5)

COPY

Parser_error_code(7:0)	Description
0xB8	ERR_FST_MBA_SKIP During MPEG operation, a macroblock has been encountered with a macro block address greater than that expected. This is likely to indicate an error in
0xB9	ERR_PICTURE_END_UNEXPECTED During MPEG operation, s PICTURE_END Token has been encountered in an unexpected place. This is likely to indicate an error in the coded data.
0xE0 . . . 0xEF	*Errors* reserved for internal test programs
0xE0	ERR_TST_PROGRAM Mysteriously arrived in the test program.
0xE1	ERR_NO_PROGRAM If the test program is not compiled in
0xE2	ERR_TST_END End of Test
0xF0...0xFF	Reserved errors
0xF0	ERR_UCODE_ADDR fell off the end of the world
0xF1	ERR_NOT IMPLEMENTED

Table A.14.12 Parser error codes (Sheet 5 of 5)

Each standard uses a different sub-set of the defined Parser error codes.

Token Name	MPEG	JPEG	H.261
ERR_NO_ERROR	✓	✓	✓
ERR_EXTENSION_TOKEN	✓	✓	
ERR_EXTENSION_DATA	✓	✓	
ERR_USER_TOKEN	✓	✓	
ERR_USER_DATA	✓	✓	
ERR_PSPARE			✓
ERR_GSPARE			✓
ERR_PTYPE			✓
ERR_JPEG_FRAME		✓	
ERR_JPEG_FRAME_LAST		✓	
ERR_JPEG_SCAN		✓	

Table A.14.13 Parser error codes and the different standards

Token Name	MPEG	JPEG	H.251
ERR_JPEG_SCAN_COMP		✓	
ERR_DNL_MARKER		✓	
ERR_MPEG_SEQUENCE	✓		
ERR_EXTRA_PICTURE	✓		
ERR_EXTRA_SLICE	✓		
ERR_VBV_DELAY	✓		
ERR_SHORT_TOKEN	✓	✓	✓
ERR_H261_PIC_END_UNEXPECTED			✓
ERR_GN_BACKUP			✓
ERR_GN_SKIP_GOB			✓
ERR_NBASE_TAB		✓	
ERR_QUANT_PRECISION		✓	
ERR_SAMPLE_PRECISION		✓	
ERR_NBASE_SCAN		✓	
ERR_UNEXPECTED_DNL		✓	
ERR_EOS_UNEXPECTED		✓	
ERR_RESTART_SKIP		✓	
ERR_SKIP_INTRA	✓		
ERR_SKIP_DINTRA	✓		
ERR_BAD_MARKER	✓		
ERR_D_MBTYPE	✓		
ERR_D_MBEND	✓		
ERR_SVP_BACKUP	✓		
ERR_SVP_SKIP_ROWS	✓		
ERR_FST_MBA_BACKUP	✓		
ERR_FST_MBA_SKIP	✓		
ERR_PICTURE_END_UNEXPECTED	✓		
ERR_TST_PROGRAM	✓	✓	✓
ERR_NO_PROGRAM	✓	✓	✓
ERR_TST_END	✓	✓	✓
ERR_UCODE_ADDR	✓	✓	✓
ERR_NOT_IMPLEMENTED	✓	✓	✓

Table A.14.13 Parser error codes and the different standards (cont'd)

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A.17.1 Temporal Decoder Signals

Signal Name	I/O	Pin Number	Description
in_data[8:0]	I	173, 172, 171, 169, 168, 167, 166, 164, 163	Input Port. This is a standard two wire interface normally connected to the Output Port of the Spatial Decoder. See sections A.4 and A.181
in_extn	I	174	
in_valid	I	162	
in_accept	O	161	
$\overline{enable}$ [1:0]	I	126, 127	Micro Processor Interface (MPI) See A.6.1. on page 69
$\overline{rw}$	I	125	
addr[7:0]	I	137, 136, 135, 133, 132, 131, 130, 128	
data[7:0]	O	152, 151, 149, 147, 145, 143, 141, 140	
irq	O	154	
DRAM_data[31:0]	I/O	15, 17, 19, 20, 22, 25, 27, 30, 31, 33, 35, 38, 39, 42, 44, 47, 49, 57, 59, 61, 63, 66 68, 70, 72, 74, 76, 79, 81, 83, 84, 85	DRAM Interface. See section A.5.2
DRAM_addr[10:0]	O	184, 186, 188, 189, 192, 193, 195, 197, 199, 200, 203	
$\overline{RAS}$	O	11	
$\overline{CAS}$ [3:0]	O	2, 4, 6, 8	
$\overline{WE}$	O	12	
$\overline{OE}$	O	204	
DRAM_enable	I	112	
out_data[7:0]	O	89, 90, 92, 93, 94, 95, 97, 98	Output Port. this is a standard two wire interface. See sections A.4
out_extn	O	87	
out_valid	O	99	
out_accept	I	100	
tck	I	115	JTAG port. See section A.8
tdi	I	116	
tdo	O	120	
tms	I	117	
$\overline{trst}$	I	121	
decoder_clock	I	177	The main decoder clock. See Table
$\overline{reset}$	I	160	Reset.

Table A.17.1 Temporal Decoder signals (contd)

COPY

Signal Name	I/O	Pin Num.	Description
tph0ish	I	122	If override = 1 then tph0ish and tph1ish are inputs for the on-chip two phase clock. For normal operation set override = 0. tph0ish and tph1ish are ignored (so connect to GND or VDD).
tph1ish	I	123	
override	I	110	
chiptest	I	111	Set chiptest = 0 for normal operation.
tloop	1	114	Connect to GND or VDD during normal operation.
ramtest	I	109	If ramtest = 1 test of the on-chip RAMs is enabled. Set ramtest = 0 for normal operation.
pllselect	I	178	If pllselect = 0 the on-chip phase locked loops are disabled.
ti	I	180	Two clocks required by the DRAM interface during test operation.
tq	I	179	
pdout	O	207	These two pins are connections for an external filter for the phase lock loop.
Pdin	1	206	

Table A.17.2 Temporal Decoder Test signals

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
nc	208	nc	156	nc	104	nc	52
test pin	207	nc	155	nc	103	nc	51
test pin	206	irq	154	nc	102	nc	50
GND	205	nc	153	VDD	101	DRAM_data[15]	49
OE	204	data[7]	152	out_accept	100	nc	48
DRAM_addr[0]	203	data[6]	151	out_valid	99	DRAM_data[16]	47
VDD	202	nc	150	out_data[0]	98	nc	46
nc	201	data[5]	149	out_data[1]	97	GND	45
DRAM_addr[1]	200	nc	148	GND	96	DRAM_data[17]	44
DRAM_addr[2]	199	data[4]	147	out_data[2]	95	nc	43
GND	198	GND	146	out_data[3]	94	DRAM_data[18]	42
DRAM_addr[3]	197	data[3]	145	out_data[4]	93	VDD	41
nc	196	nc	144	out_data[5]	92	nc	40

Table A.17.3 Temporal Decoder Pin Assignments

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A.17.1.4 - JTAG pins for normal operation

See Section A.8.1

Addr. (hex)	Register Name	See table
0x00 . . . 0x01	Interrupt service area	A.17.6
0x02 . . . 0x07	Not used	
0x08	Chip access	A.17.7
0x09 . . . 0x0F	Not used	
0x10	Picture sequencing	A.17.8
0x11 . . . 0x1F	Not used	
0x20 . . . 0x2E	DRAM interface configuration registers	A.17.9
0x2F . . . 0x3F	Not used	
0x40 . . . 0x53	Buffer configuration	A.17.10
0x54 . . . 0x5F	Not used	
0x60 . . . 0xFF	Test registers	A.17.11

Table A.17.5 Overview of Temporal Decoder memory map

Addr. (hex)	Bit num.	Register Name	Page references
0x00	7	chip_event	
	6:2	not used	
	1	chip_stopped_event	
	0	count_error_event	
0x01	7	chip_mask	
	6:2	not used	
	1	chip_stopped_mask	
	0	count_error_mask	

Table A.17.6 Interrupt service area registers

COPY

Addr. (hex)	Bit num.	Register Name	Page references
0x08	7:1	not used	
	0	chip_access	

Table A.17.7 Chip access register

Addr. (hex)	Bit num.	Register Name	Page references
0x10	7:1	not used	
	0	MPEG_reordering	

Table A.17.8 Picture sequencing

COPY

Addr. (hex)	Bit num.	Register Name	Page references
0x20	7:5	not used	
	4:0	page_start_length(4:0)	
0x21	7:4	not used	
	3:0	read_cycle_length(3:0)	
0x22	7:4	not used	
	3:0	write_cycle_length(3:0)	
0x23	7:4	not used	
	3:0	refresh_cycle_length(3:0)	
0x24	7:4	not used	
	3:0	CAS_falling(3:0)	
0x25	7:4	not used	
	3:0	RAS_falling(3:0)	
0x26	7:1	not used	
	0	interface_timing_access	
0x27	7:0	not used	
0x28	7:6	RAS_strength(2:0)	
	5:3	OEWE_strength(3:0)	
	2:0	DRAM_data_strength(3:0)	
0x29	7	not used	
	6:4	DRAM_addr_strength(3:0)	
	3:1	CAS_strength(3:0)	
	0	RAS_strength(3)	

Table A.17.9 DRAM interface configuration registers

COPY

Addr. (hex)	Bit num.	Register Name	Page references
0x28	7	not used	
	6:4	DRAM_addr_strength[3:0]	
	3:1	CAS_strength[3:0]	
	0	RAS_strength[3]	
0x29	7:6	RAS_strength[2:0]	
	5:3	OEWE_strength[3:0]	
	2:0	DRAM_data_strength[3:0]	
0x2A	7:0	refresh_interval	
0x2B	7:0	not used	
0x2C	7:6	not used	
	5	DRAM_enable	
	4	no_refresh	
	3:2	row_address_bits[1:0]	
	1:0	DRAM_data_width[1:0]	
0x2D	7:0	not used	
0x2E	7:0	Test registers	

Table A.17.9 DRAM interface configuration registers (contd)

Addr. (hex)	Bit num.	Register Name	Page references
0x40	7:0	not used	
0x41	7:2		
	1:0	picture_buffer_0[17:0]	
0x42	7:0		
0x43	7:0		
0x44	7:0	not used	
0x45	7:2		
	1:0	picture_buffer_1[17:0]	
0x46	7:0		
0x47	7:0		

Table A.17.10 Buffer configuration registers

COPY

Addr. (hex)	Bit num.	Register Name	Page references
0x48	7:0	not used	
0x49	7:1		
	0	component_offset_0[16:0]	
0x4A	7:0		
0x4B	7:0		
0x4C	7:0	not used	
0x4D	7:1		
	0	component_offset_1[16:0]	
0x4E	7:0		
0x4F	7:0		
0x50	7:0	not used	
0x51	7:1		
	0	component_offset_2[16:0]	
0x52	7:0		
0x53	7:0		

Table A.17.10 Buffer configuration registers (contd)

Addr. (hex)	Bit num.	Register Name	Page references
0x2E	7 ... 4	PLL resistors	
	3 ... 0		
0x60	7 ... 6	not used	
	5 ... 4	coding_standard[1:0]	
	3 ... 2	picture_type[1:0]	
	1	H261_filt	
	0	H261_s_f	
0x61	7 ... 6	component_id	
	5 ... 4	prediction_mode	
	3 ... 0	max_sampling	
0x62	7 ... 0	samp_h	
0x63	7 ... 0	samp_v	

Table A.17.11 Test registers

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Addr. (hex)	Bit num.	Register Name	Page references
0x64	7 ... 0	back_h	
0x65	7 ... 0		
0x66	7 ... 0	back_v	
0x67	7 ... 0		
0x68	7 ... 0	forw_h	
0x69	7 ... 0		
0x6A	7 ... 0	forw_v	
0x6B	7 ... 0		
0x6C	7 ... 0	width_in_mb	
0x6D	7 ... 0		

Table A.17.11 Test registers (contd)